Vegas Schematic

SKL/KBL-U

2016/06/27

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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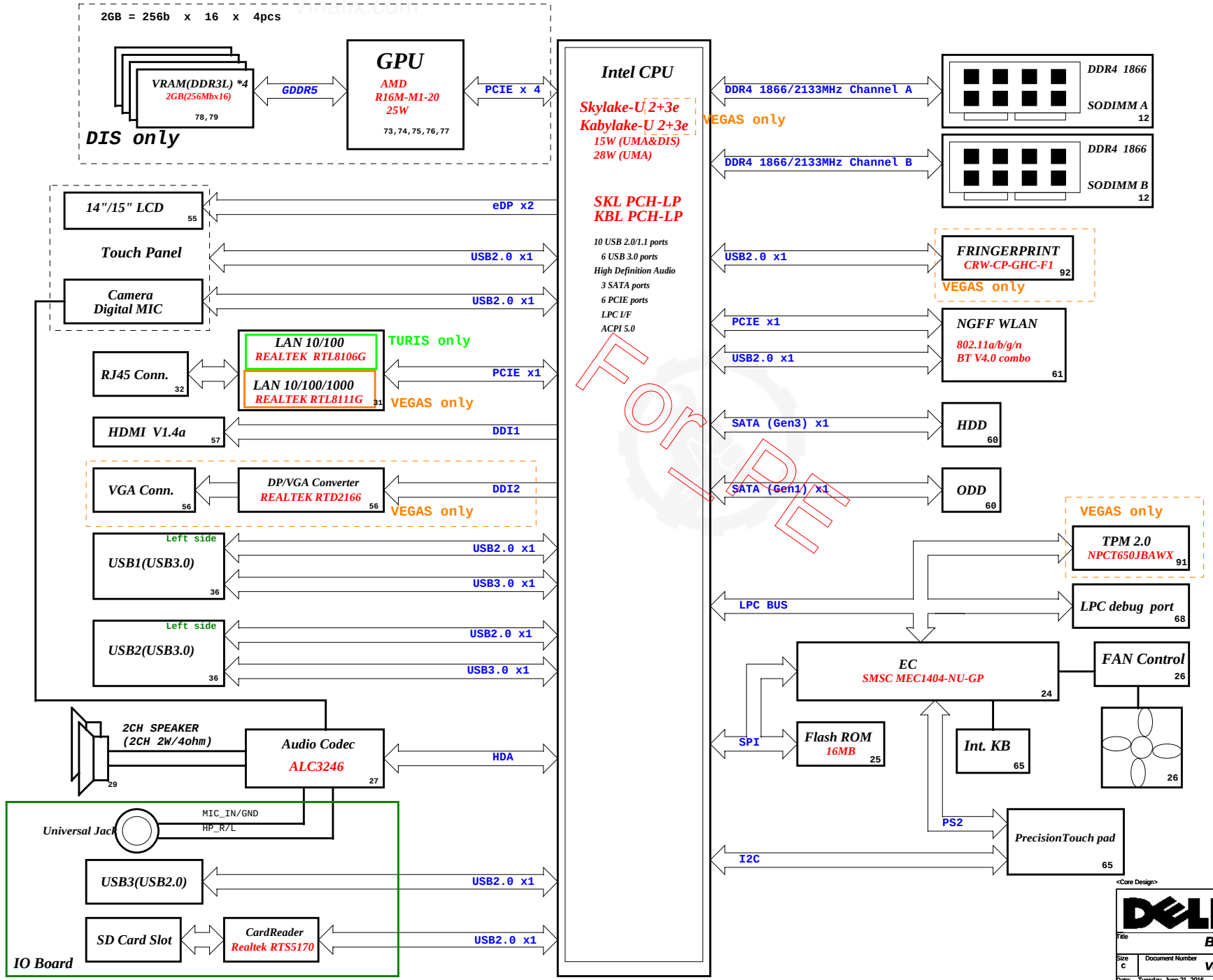
Title: ***Cover Page***		
Size: A4	Document Number: **Vegas SKL/KBL-U**	Rev: **A00**
Date: Monday, June 27, 2016	Sheet 1 of 105	

Project code:4PD09P010001
PCB P/N: 15341-SD
Revision: A00

Vegas SKL-U/KBL-U Block Diagram



CHARGER		
ISL88739		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power	
NCP81208MNTXG	46~50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS	
RT8231AGQW-GP APL5930KAI-TRG	51
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V	
	11
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A	
AOZ2262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE	
ISL62771HRTZ-GP-U	85
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

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Title: Block Diagram

Size	Document Number	Rev
C	Vegas SKL/KBL-U	A00

Date: Tuesday, June 21, 2016 Sheet 2 of 105

(Blanking)

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Title
(Reserved)

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 3 of 105

Main Func = CPU

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

R401 1KR2J-1-GP (Rb)
R403 499R2F-2-GP (Ra)
R419 1KR2J-1-GP
R420 0R2J-2-GP

TP401 TPAD14-OP-GP
TP402 TPAD14-OP-GP
TP403 TPAD14-OP-GP
TP404 TPAD14-OP-GP
TP405 TPAD14-OP-GP
TP406 TPAD14-OP-GP
TP407 TPAD14-OP-GP
TP408 TPAD14-OP-GP

R410 0R0402-PAD

CPU1D 4 OF 20
SKYLAKE_ULT
SKYLAKE-U-GP

CPU MISC: CATERR#, PECI, PROCHOT#, THERMTRIP#, SKTOCC#, BPM#[0], BPM#[1], BPM#[2], BPM#[3], GPP_E3/CPU_GP0, GPP_E7/CPU_GP1, GPP_B3/CPU_GP2, GPP_B4/CPU_GP3, PROC_POPIRCOMP, PCH_OPIRCOMP, OPCE_RCOMP, OPC_RCOMP

JTAG: PROC_TCK, PROC_TDI, PROC_TDO, PROC_TMS, PROC_TRST#, PCH_JTAG_TCK, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_TMS, PCH_TRST#, JTAGX

071.SKYLA.000U

R412 R413 R414 R415 49D9R2F-GP

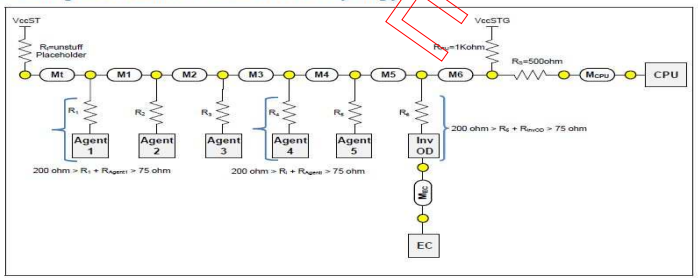
+VCCSTG = 1.0 V

R421 R422 R423 R408 R409 R416 R417 R402 R406 R407 51R2J-2-GP, 100R2J-2-GP, 1KR2J-1-GP

EC401 SC1KP50V2KX-1GP

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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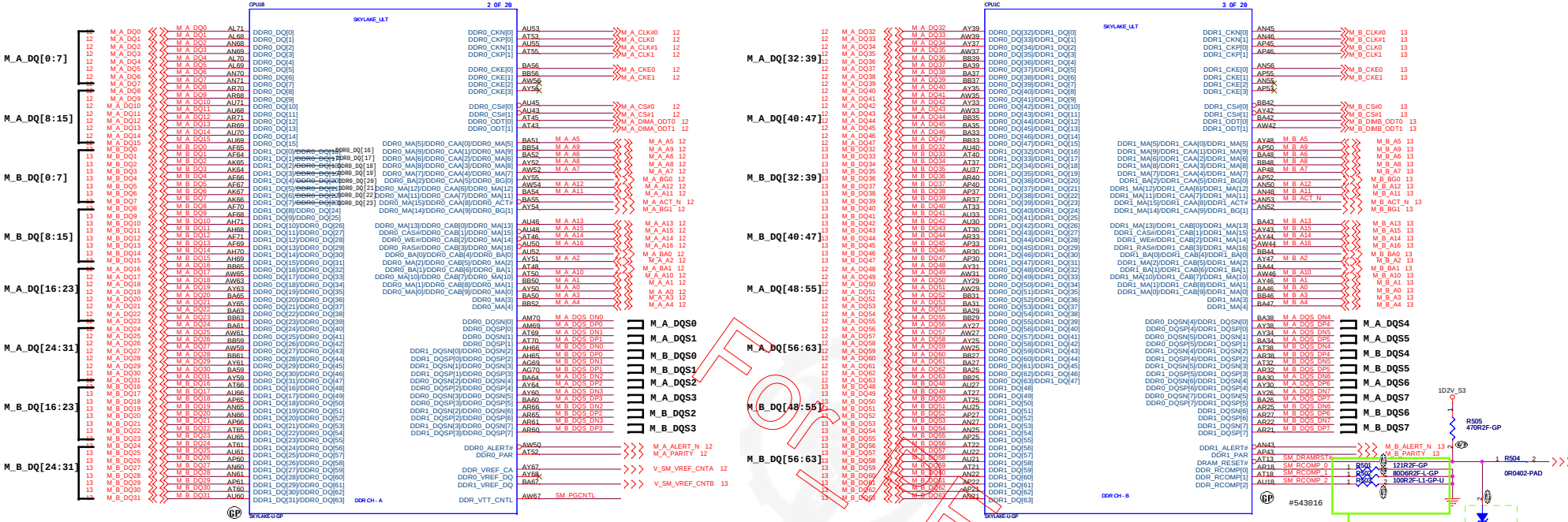
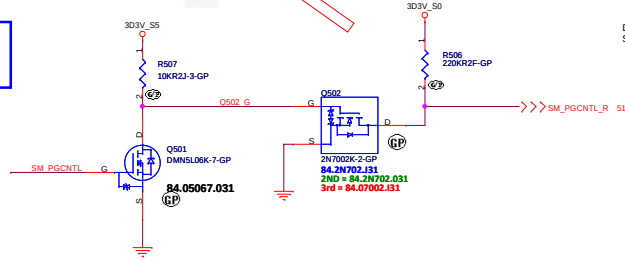
Title: CPU_(JTAG/CPU SIDE BAND)
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 4 of 105

Main Func = CPU

DDR4 ball type: Interleaved Type



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Layout Note:

PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT.	3,4
		DRAMs	ODT[1:0]	Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

<Core Design>

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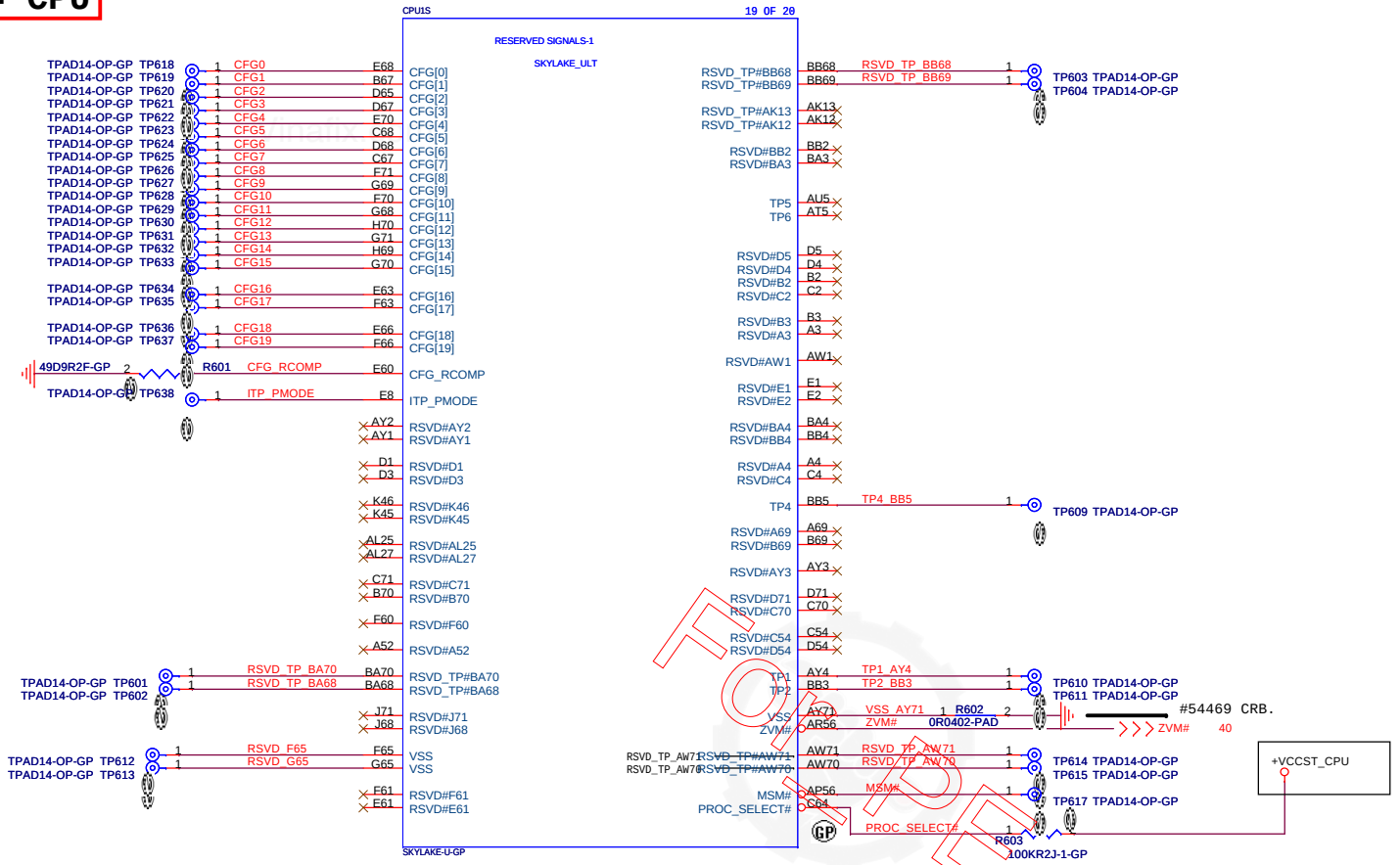
Title: CPU (DDR)

Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

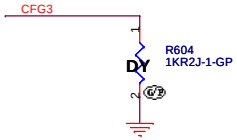
Date: Monday, June 27, 2016 Sheet 5 of 105

Main Func = CPU



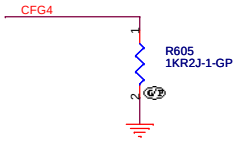
PCH strap pin:

071.SKYLA.000U



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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Title: CPU (RESERVED)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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Main Func = CPU

140mA

3A

3A

071.SKYLA.000U

071.SKYLA.000U

for 2+3E

071.SKYLA.000U

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

RN701 RN702 change to Single for cost change 2/26

SVID_543016:

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology

SVID DATA

SVID CLOCK

<Core Design>

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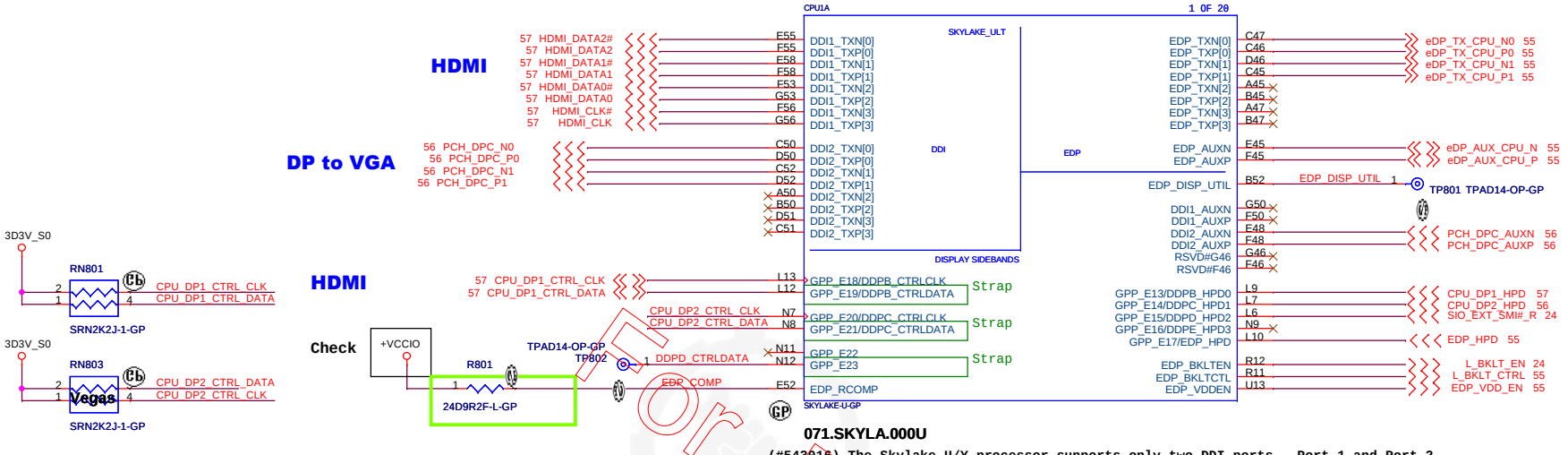
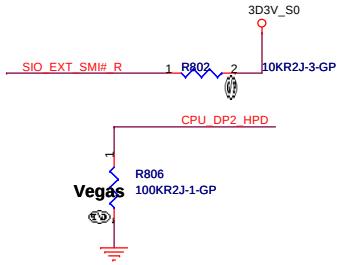
Title: CPU(VCC_CORE)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 7 of 105

Main Func = CPU





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU (DISPLAY)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 8 of 105

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

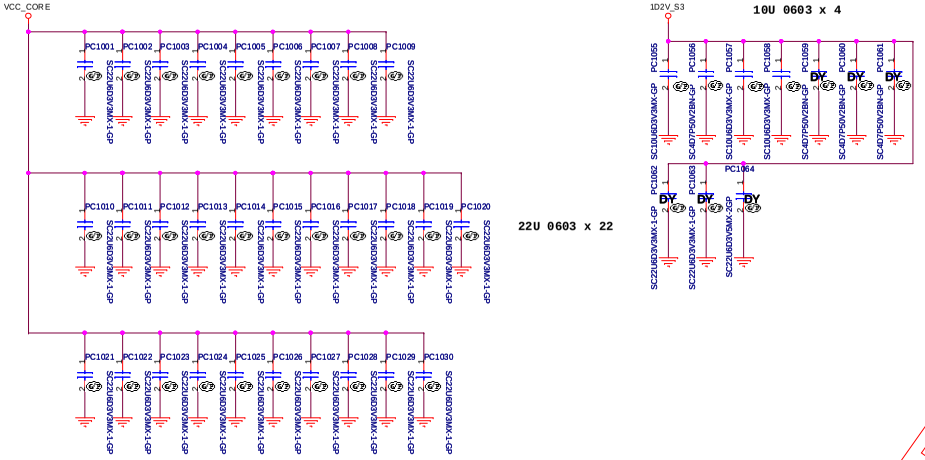
Date: Thursday, June 16, 2016 Sheet 9 of 105

Main Func = CPU

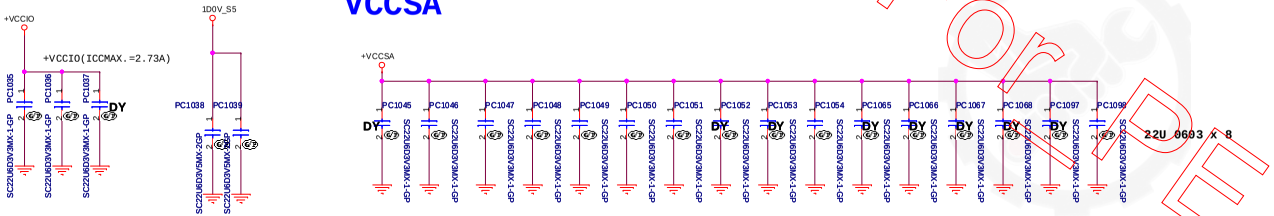
(#543016 PDG)

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A



VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

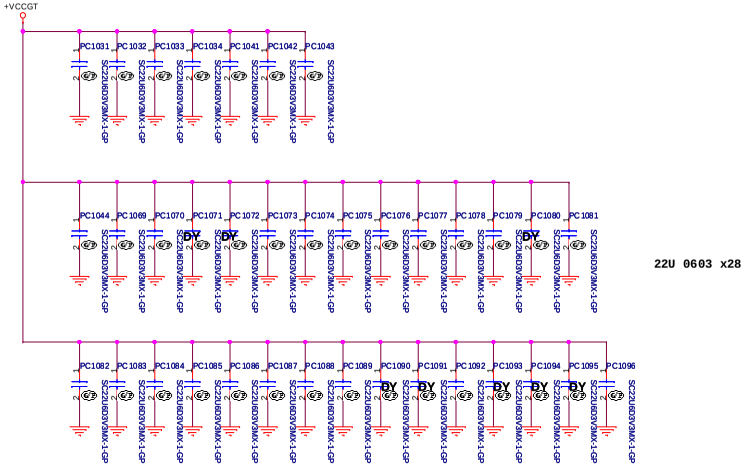


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

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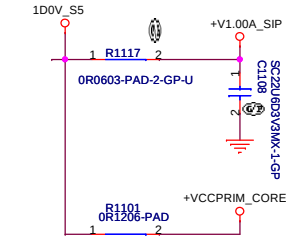
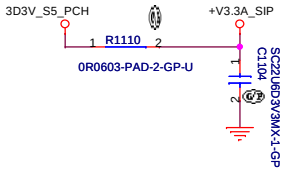
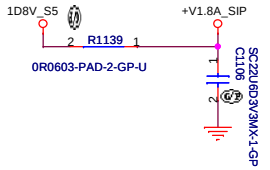
Title: CPU (Power CAP1)
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Thursday, June 16, 2016 | Sheet 10 of 105

Main Func = CPU

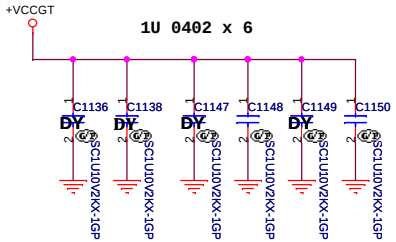
PCH DERIVED RAILS



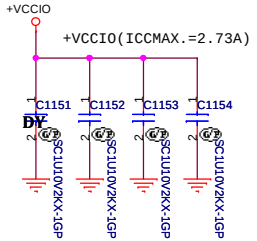


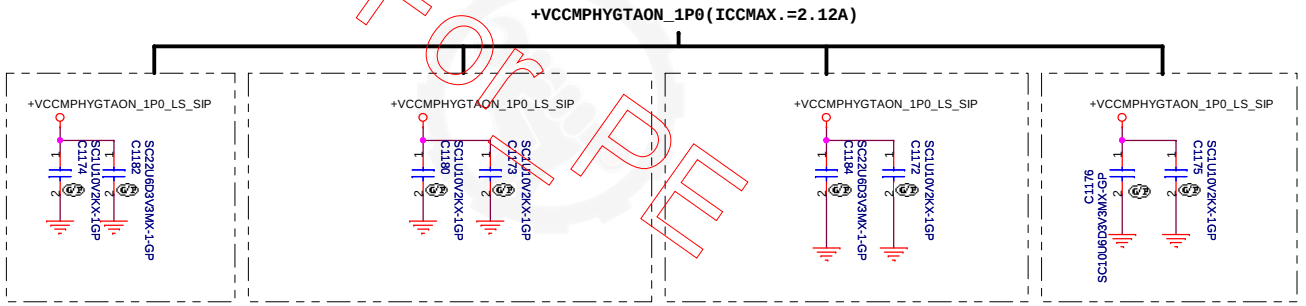


UNSLICED GT



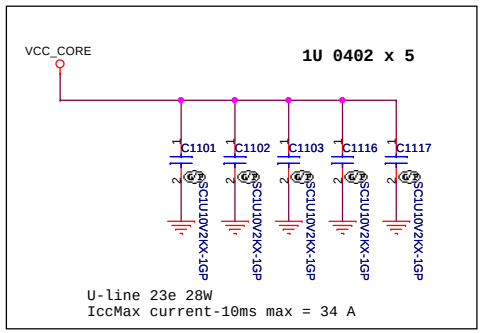
VCCIO

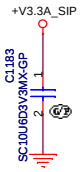


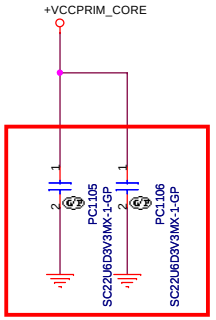


Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15





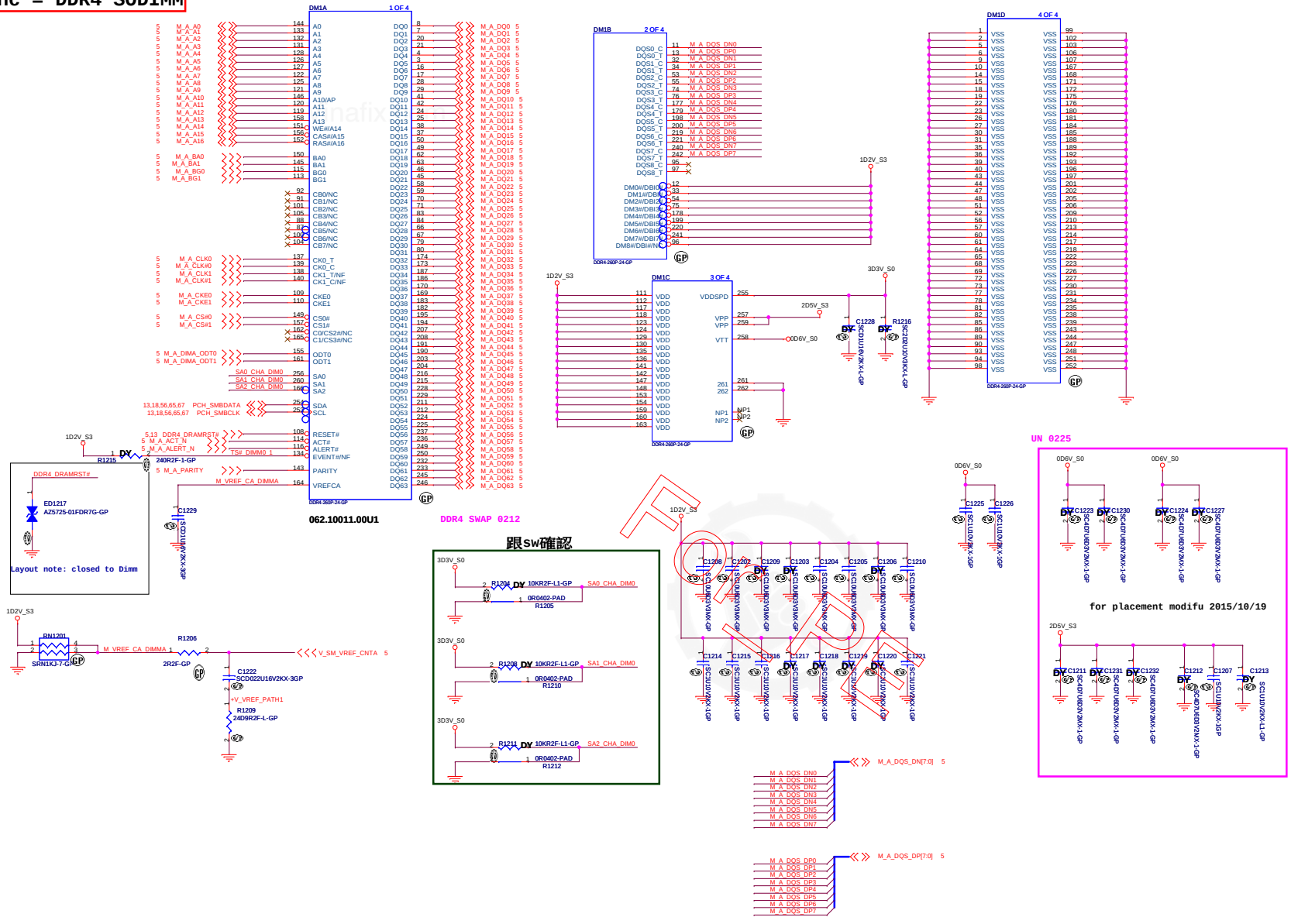


<Core Design>

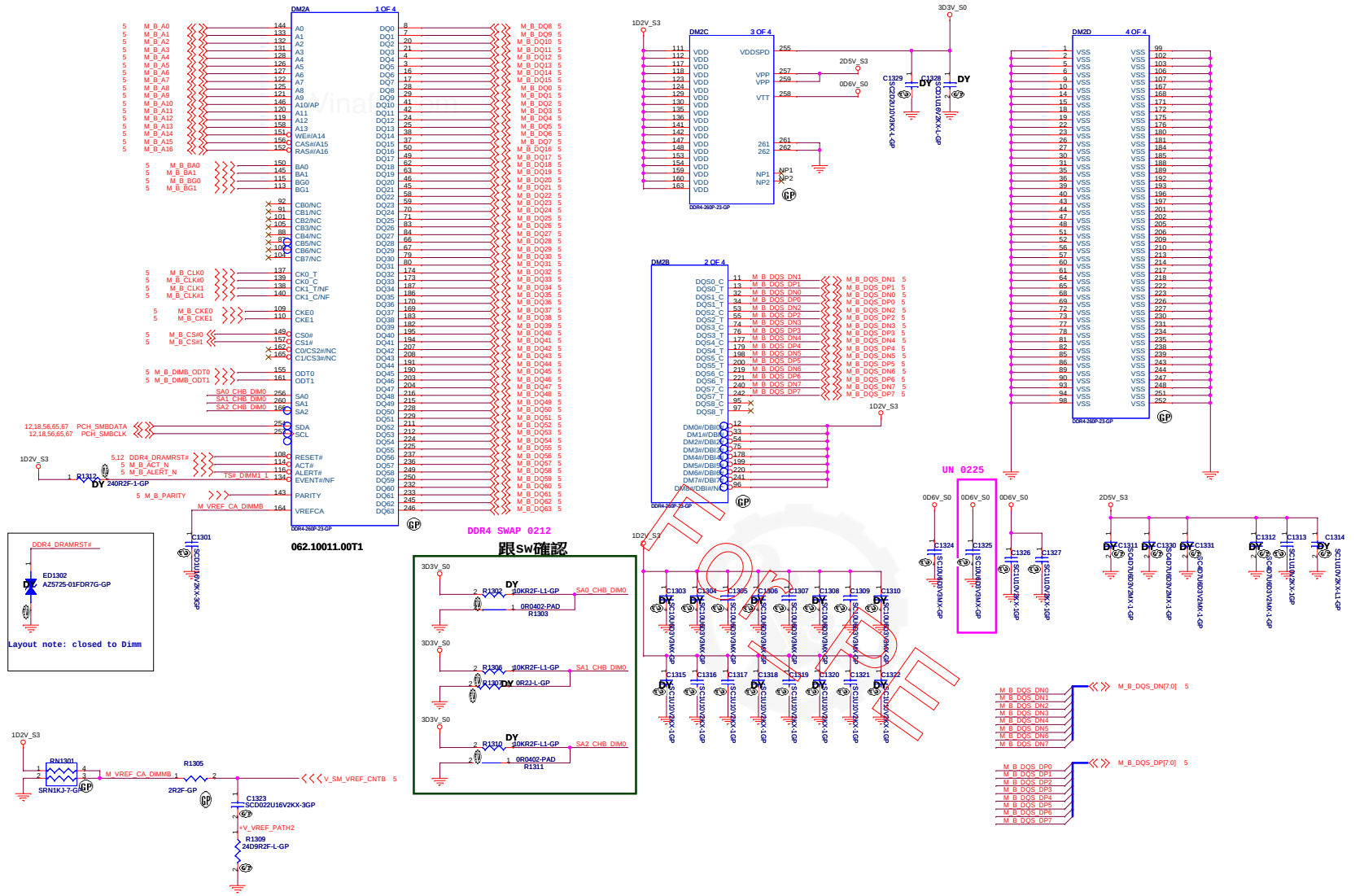
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (Power CAP2)	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Friday, June 24, 2016	Sheet 11 of 105	

Main Func = DDR4 SODIMM



Main Func = DDR4 SODIMM



Title: DDR3-SODIMM1

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 13 of 106

(Blanking)

<Core Design>

Wistron Corporation
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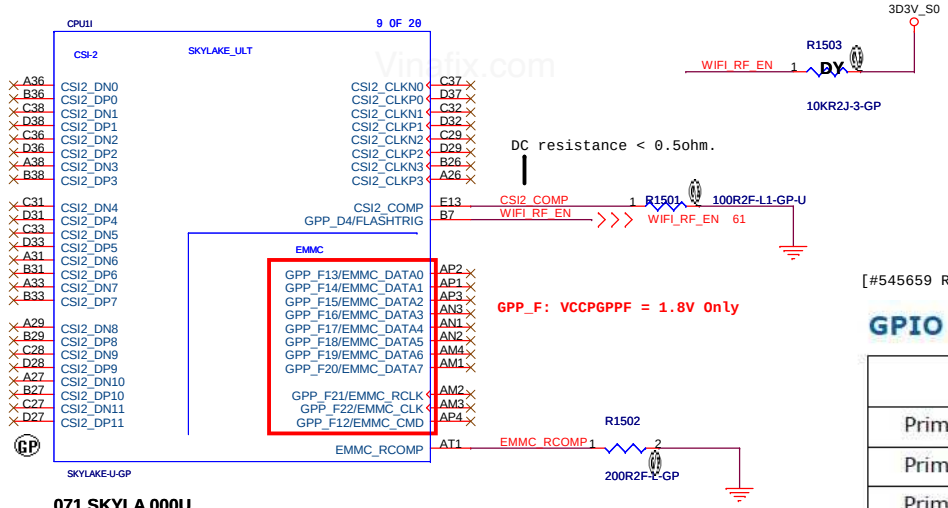
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 14 of 105

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

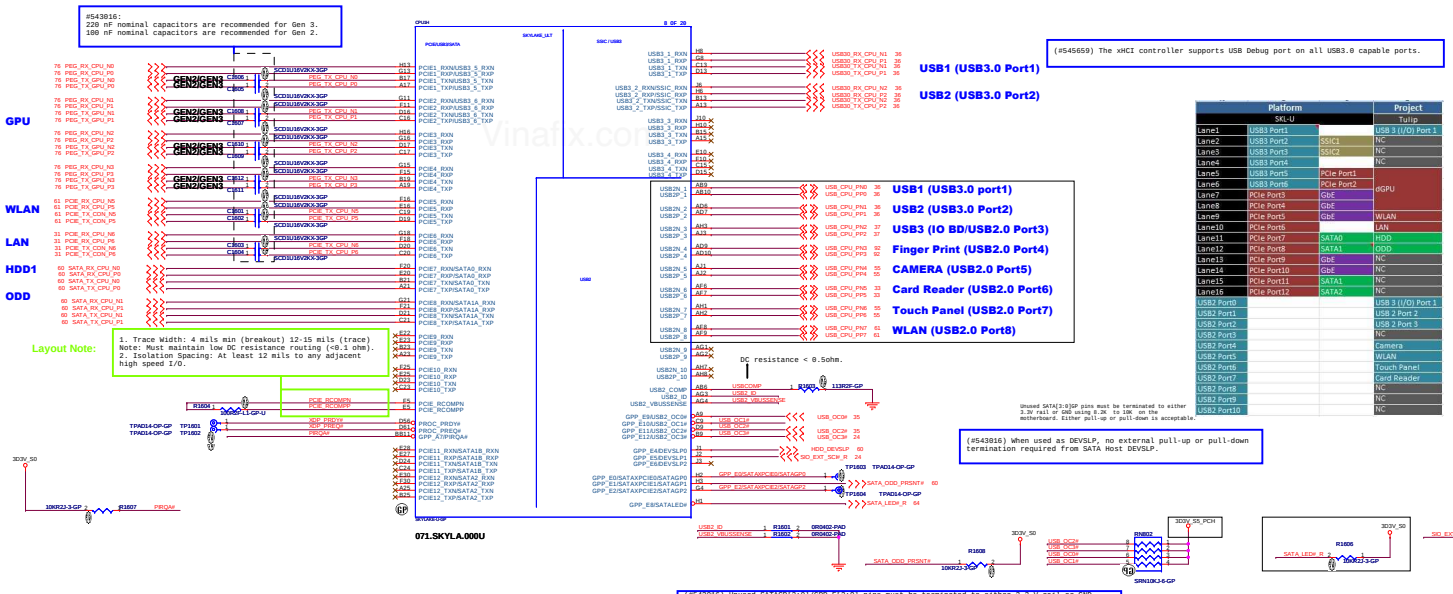
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 15 of 105



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger Print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

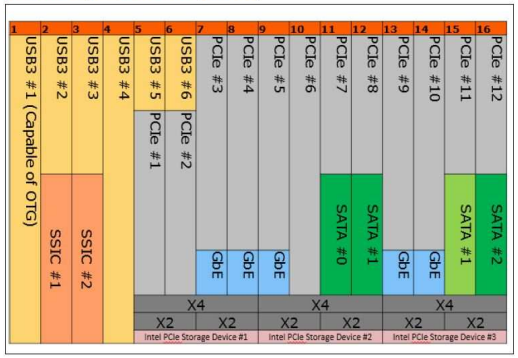


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH

3D3V_S5 — RN1704 — AC_PRESENT, PCH_WAKE#, PCH_BATLOW#, GPD11/LANPHYPC — SRN10KJ-6-GP

GPD11 pull high by Intel PDG1.3 request

BATLOW#:
Pull-up required even if not implemented.

3D3V_S5 — R1711 0R0603-PAD — +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 — #544669 (CRB): 330k. — R1730 330KR2J-L1-GP — SM_INTRUDER#

3D3V_S5_PCH — R1731 20KR2J-L2-GP — EXT_PWR_GATE# — R1718 10KR2J-3-GP — ME_SUS_PWR_ACK_R

RN1701 — PM_RSMRST#, PM_PCH_PWROK — SRN10KJ-5-GP — R1717 10KR2J-3-GP — SYS_PWROK

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

H_CPUPWRGD — R405 10KR2J-3-GP

DY for OBFF disable

+VCCPDSW_3P3 — R1707 10KR2J-3-GP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

24 EC_WAKE# — R1710 0R0402-PAD — GPD2/LAN_WAKE#

24,31,40,55,61,68,76,91 PLT_RST# — R1713 0R0402-PAD — PCH_PLTRST#

+V3.3A_SIP — R1701 10KR2J-3-GP

R1715 100KR2J-1-GP — C1701 SC220P50V2KX-3GP

CPU1K — 11 OF 20 — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT

TPAD14-OP-GP TP1710 — XDP_DBRESET# — PM_RSMRST# — PCH_PLTRST#

40 H_THERMTRIP_EN — 0R2J-2-GP R1734 — H_VCCST_PWRGD_R — 60D4R2F-GP R1734 — H_VCCST_PWRGD — H_CPUPWRGD

24 SYS_PWROK — 24,26,40 RESET_OUT# — R1706 0R0402-PAD — R1704 0R2J-2-GP — PM_RSMRST# — PM_PCH_PWROK — PCH_DPWROK — SYS_PWROK

ME_SUS_PWR_ACK_R — SUSACK# R — PCH_WAKE# — GPD2/LAN_WAKE# — GPD11/LANPHYPC

GPP_B13/PLTRST# — SYS_RESET# — RSMRST# — PROCPWRGD — VCCST_PWRGD — SYS_PWROK — PCH_PWROK — DSW_PWROK — GPP_A13/SUSWARN#/SUSPWRDNACK — GPP_A15/SUSACK# — WAKE# — GPD2/LAN_WAKE# — GPD11/LANPHYPC — GPD7/RSVD#AT15

GPP_B12/SLP_S0# — GPD4/SLP_S3# — GPD5/SLP_S4# — GPD10/SLP_S5# — SLP_SUS# — SLP_LAN# — GPD9/SLP_WLAN# — GPD6/SLP_A# — GPD3/PWRBTN# — GPD1/ACPRESENT — GPD0/BATLOW# — GPP_A11/PME# — INTRUDER# — GPP_B11/EXT_PWR_GATE# — GPP_B2/VRALERT#

SIO_SLP_S0# — TP17011 TPAD14-OP-GP — SIO_SLP_S3# 24,27,40,51 — SIO_SLP_S4# 24,40,44,51

SIO_SLP_SUS# — TP17032 TPAD14-OP-GP
SIO_SLP_LAN# — TP17042 TPAD14-OP-GP
GPD9/SLP_WLAN# — TP17052 TPAD14-OP-GP
SIO_SLP_A# — TP17062 TPAD14-OP-GP

AC_PRESENT — SIO_PWRBTN# 24
PCH_BATLOW#
PM# — SM_INTRUDER# — TP17071 TPAD14-OP-GP
EXT_PWR_GATE#

SKYLAKE-U-GP

071.SKYLA.000U

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

AC_PRESENT — EC1707 SCD01U16V2KX-3GP

+VCCMPHYGTAON_1P0

SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

1D0V_S5 — R1724 0R0805-PAD — +VCCMPHYGTAON_1P0_LS_SIP — R1735 0R0805-PAD — C1704 SC10U6D3V3MX-GP

3D3V_S5 — U1702 U74LVC1G07G-AL5-R-GP — 73.01G07.AHG — C1703 SCD01U25V2KX-3GP — 24,27,40,51 SIO_SLP_S3#

3D3V_S5 +VCCSTG — C1702 SCD01U50V2KX-3GP — R1722 100KR2J-1-GP

24,40 ALL_SYS_PWRGD — U1701 U74LVC1G07G-AL5-R-GP — 73.01G07.AHG — H_VCCST_PWRGD_R

EC1708 SCD01U50V2KX-1GP

R1716 100KR2F-L1-GP — R1719 47KR2F-GP — EC1709 SCD1U16V2KX-3GP

XDP_DBRESET# — SYS_PWROK — PLT_RST# — RESET_OUT# — 3V_5V_POK

EC1706 EC1702 EC1703 SC10P50V2KX-1GP — EC1705 EU1101 AZ5325-01FDF7G-GP — EC1704 SC1P50V2KX-1GP

3D3V_AUX_S5 — D1702 RB751V-40H-GP — 83.R2004.G8F — ACOK_IN 24,44

R1737 100KR2J-1-GP — PM_RSMRST# M — Q1702 NON DS3 — 2N7002KDW-GP — AC_PRESENT — PM_RSMRST#

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

ME_SUS_PWR_ACK_R — R1708 0R0402-PAD — SUSACK# R

24 ME_SUS_PWR_ACK — R1709 0R0402-PAD — ME_SUS_PWR_ACK_R

3D3V_AUX_S5 — R1727 100KR2J-1-GP — NON DS3 — R1726 10KR2J-3-GP — Q1701 2N7002KDW-GP

3V_5V_POK# — PM_RSMRST# — 1KR2J-1-GP R1702 — 3V_5V_POK_C — R1728 0R0402-PAD — 3V_5V_POK 40,45,53,54 — PCH_RSMRST# 24

EC1712 SCD1U16V2KX-3GP

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 17 of 105

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH Prim

3D3V_S5_PCH

R1822 1KR2J-1-GP

GPP_C5/SML0ALERT#

R1823 1KR2J-1-GP

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH Prim

3D3V_S5_PCH

R1824 1KR2J-1-GP

SPI_SI_CPU

R1825 1KR2J-1-GP

R1835 and R1834 merge to RN1802
Follow Starlord

3D3V_S5_PCH

RN1802 SRN1KJ-7-GP

SPI_HOLD_ROM
SPI_WP_ROM

3D3V_S5_PCH

SML1_SMBDATA
SML1_SMBCLK
SML0_SMBDATA
SML0_SMBCLK

RN1807 SRN2K2J-4-GP

GPP_B23/SML1ALERT#

R1820 150KR2F-L-GP

GPP_C2/SMBALERT#

R1821 2K2R2J-2-GP

SRN2K2J-1-GP

MEM_SMBCLK
MEM_SMBDATA

RN1811

24,68,91 LPC_LAD[3..0]

LPC_LAD[3..0]

LPC_LAD2
LPC_LAD1
LPC_LAD3
LPC_LAD0

RN1806 SRN0J-7-GP-U

LPC_LAD2_R
LPC_LAD1_R
LPC_LAD3_R
LPC_LAD0_R

3D3V_S0

R2021 10KR2J-3-GP

SIO_RCIN#

R2032 10KR2J-3-GP

SERIRQ

SERIRQ PH:
PDG: 8.2k
CRB: 10k

Resister value will check later

24,25 SPI_CLK_ROM	0R0402-PAD	R1806	SPI_CLK_CPU	AV2
24,25 SPI_SO_ROM	0R0402-PAD	R1807	SPI_SO_CPU	AW3
24,25 SPI_SI_ROM	0R0402-PAD	R1808	SPI_SI_CPU	AV3
25 SPI_WP_ROM	0R0402-PAD	R1809	SPI_WP_CPU	AW2
25 SPI_HOLD_ROM	0R0402-PAD	R1811	SPI_HOLD_CPU	AU4
24,25 SPI_CS_ROM_N0	0R0402-PAD	R1812	SPI_CS_CPU_N0	AU3

CPU1E 5 OF 20

SPI - FLASH

SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

Strap

SKYLAKE_ULT

SMBUS, SMLINK

GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

MEM_SMBCLK
MEM_SMBDATA
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA

SML1_SMBCLK 24,79
SML1_SMBDATA 24,79

SUS_STAT#/LPCPD#

3D3V_S5_PCH

R1814 10KR2J-3-GP

3D3V_S0

R1818 8K2R2F-1-GP

CLKRUN# R

SPI - TOUCH

GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

CLINK

CL_CLK
CL_DATA
CL_RST#

LPC

GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#

LPC_LAD0_R
LPC_LAD1_R
LPC_LAD2_R
LPC_LAD3_R
LPC_LFRAME# R

R1801 0R0402-PAD

LPC_LFRAME# 24,68,91
SUS_STAT#/LPCPD# 91

GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

PCI_CLK_LPC1
CLKRUN# R

R1816 0R2J-2-GP

PCI_CLK_LPC0 91
CLKRUN# 24,91

GPP_A0/RCIN#
GPP_A6/SERIRQ

SKYLAKE-U-GP

071.SKYLA.000U

67 HDD_FALL_INT

0V1 add FFS 2718

TPAD14-OP-GP TP1801 CPU_D1_TP M2
TPAD14-OP-GP TP1803 CPU_D3_TP M3
TPAD14-OP-GP TP1804 CPU_D4_TP J4
TPAD14-OP-GP TP1805 CPU_D5_TP V1
TPAD14-OP-GP TP1806 CPU_D6_TP V2
CPU_D7_TP M1

61 CL_CLK
61 CL_DATA
61 CL_RST#

RCIN#:
Frequency to Avoid: 33 MHz

24 SIO_RCIN#
24,91 SERIRQ

SCD1U16V2KX-3GP

20140820 DAIVD

3D3V_S0

2N7002KDW-GP Q1801

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

MEM_SMBDATA
MEM_SMBCLK

RN1810 SRN10KJ-5-GP

3D3V_S0

PCH_SMBDATA 12,13,56,65,67
PCH_SMBCLK 12,13,56,65,67

PCI_CLK_LPC0
PCI_CLK_LPC1

R1804 LPC 0R2J-2-GP
R1805 0R0402-PAD

CLK_PCI_LPC 68
CLK_PCI_LPC_MEC 24

SCD1U16V2KX-4GP

3D3V_S0

RN1812 SRN10KJ-6-GP

CLKREQ_PCIE#5
CLKREQ_PEG#0
CLKREQ_PCIE#1
CLKREQ_PCIE#2

RN1813 SRN10KJ-5-GP

CLKREQ_PCIE#3
CLKREQ_PCIE#4

RTC_X1
RTC_X2

R1815 10MR2J-L-GP

X1802 XTAL-32D768KHZ-68-GP

82.30001.G01

2rd = 82.30001.G11

C1804 SC3D9P50V2CN-1GP
C1803 SC3D9P50V2CN-1GP

XTAL24_IN
XTAL24_OUT

R1810 0R0402-PAD
R1802 1MR2J-1-GP

X1801 XTAL-24MHZ-81-GP

82.30004.841

C1801 SC15P50V2JN-2-GP
C1802 SC15P50V2JN-2-GP

GPU
WLAN
LAN

76 PEG_CLK_CPU#
76 PEG_CLK_CPU
79 CLKREQ_PEG#0

61 PEG_CLK1_CPU#
61 PEG_CLK1_CPU
61 CLKREQ_PCIE#1

31 PEG_CLK2_CPU#
31 PEG_CLK2_CPU
31 CLKREQ_PCIE#2

CPU1J 10 OF 20

CLOCK SIGNALS

SKYLAKE_ULT

CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P

PCIE_CLK_XDP_N
PCIE_CLK_XDP_P

TP1807 TPAD14-OP-GP
TP1808 TPAD14-OP-GP

GPD8/SUSCLK

SUSCLK_R

R1813 0R0402-PAD

SUS_CLK 24

XTAL24_IN
XTAL24_OUT

XCLK_BIASREF

+V1.00A_SIP

R1903 2K7R2F-GP

Intel recommend: 2.71k ohm 5%

RTCX1
RTCX2

RTC_X1
RTC_X2

SRTCRST#
RTCRST#

SRTC_RST#
RTC_RST#

SKYLAKE-U-GP

071.SKYLA.000U

24 RTCRST_ON

R1902 10KR2J-3-GP-S

Q1901 2N7002K-2-GP

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

(#514849)

G1901 GRN-OP-GP

RTC_AUX_S5

RN1901 SRN20KJ-1-GP

SUSCLK_R

EC1803 SC407R5V2BK-GP

SRTC_RST#
RTC_RST#

SCD1U16V2KX-3GP

C1902 SC1U10V2KX-1GP

SCD1U10V2KX-3GP

SCD1U16V2KX-3GP

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

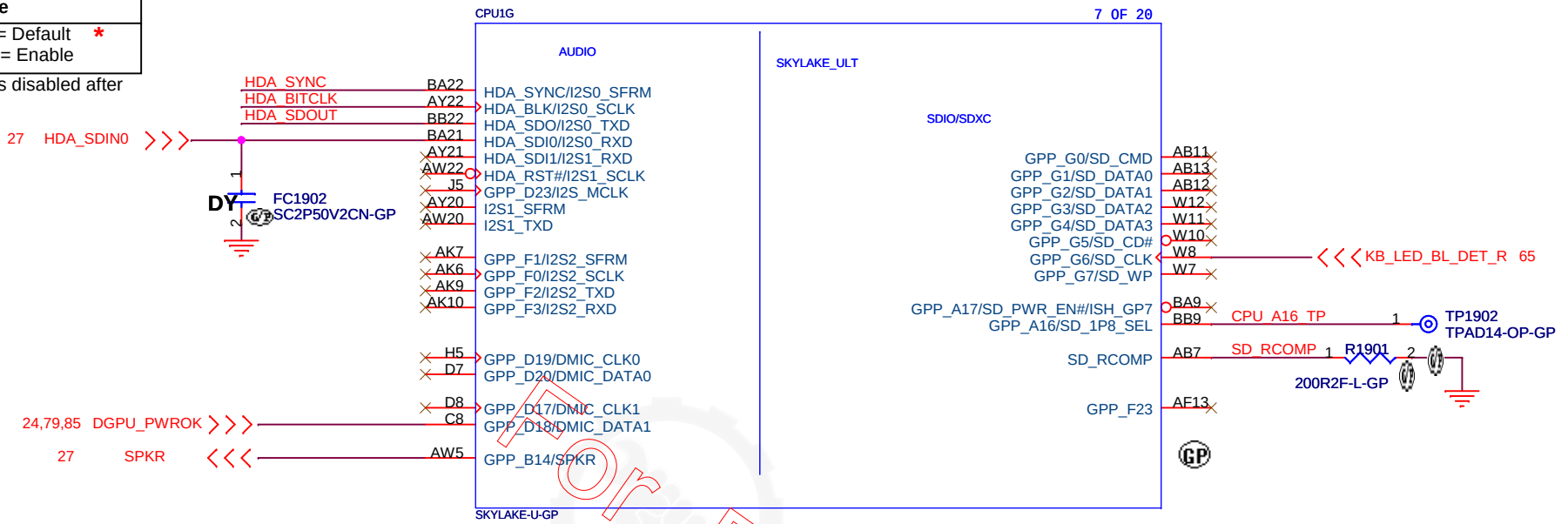
Date: Monday, June 27, 2016 | Sheet 18 of 105

Main Func = PCH

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

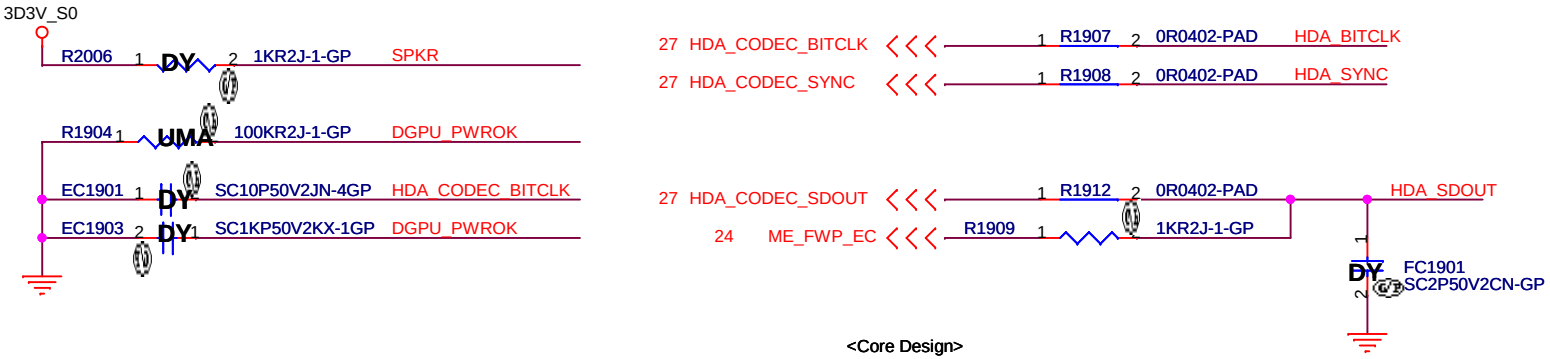


071.SKYLA.000U

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_(AUDIO/SDIO/SDXC)**

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 19 of 105

Main Func = PCH

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

071.SKYLA.000U

For debug USB/UART:

Intel has removed EHCI controller from BDW and proposed to use UART interface for Win7 debug.

BIOS strap pin:

GPP_A19 GPP_A18

PROJECT Strap pin	PROJECT_ID2	PROJECT_ID1
Turis	X	0
Vegas	X	1
KBL	0	X
SKL	1	X

BIOS strap pin:

GPP_C11

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

GPP_A22

BIOS UMA/DIS Strap pin	TPM_SELECT
TPM	1
NON_TPM	0

BIOS strap pin:

GPP_B17

BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

<Core Design>

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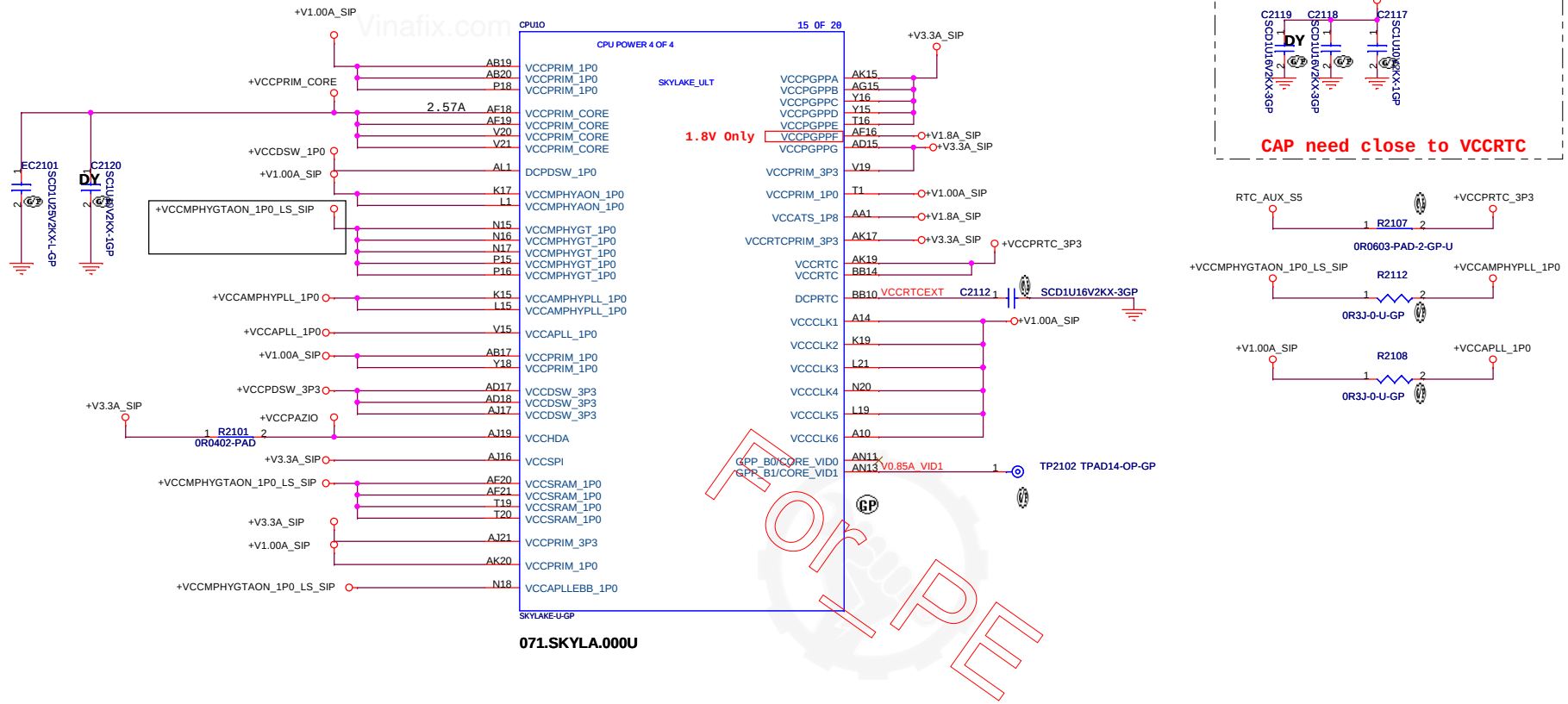
Taipei Hsien 221, Taiwan, R.O.C.

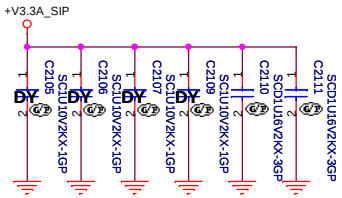
Title: CPU (LPSS/ISH)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

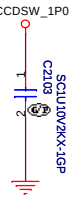
Date: Monday, June 27, 2016 | Sheet 20 of 105

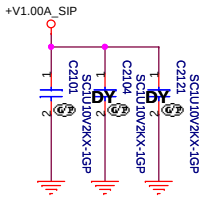
Main Func = PCH



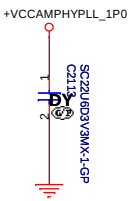


Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

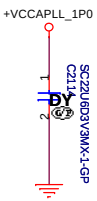




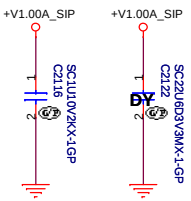
Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1



Layout Note:
22uF:
C2113 near K15



Layout Note:
22uF:
C2113 near K15



Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

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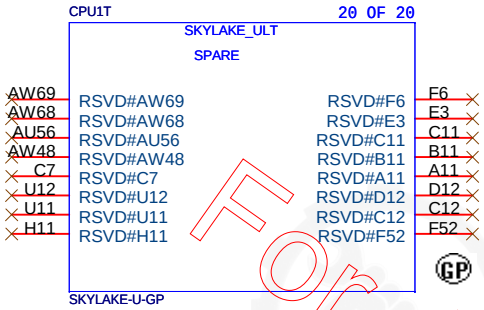
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size	Document Number	Rev
A3	Vegas SKL/KBL-U	A00

Date: Friday, June 24, 2016 Sheet 21 of 105

Main Func = PCH



071.SKYLA.000U

<Core Design>

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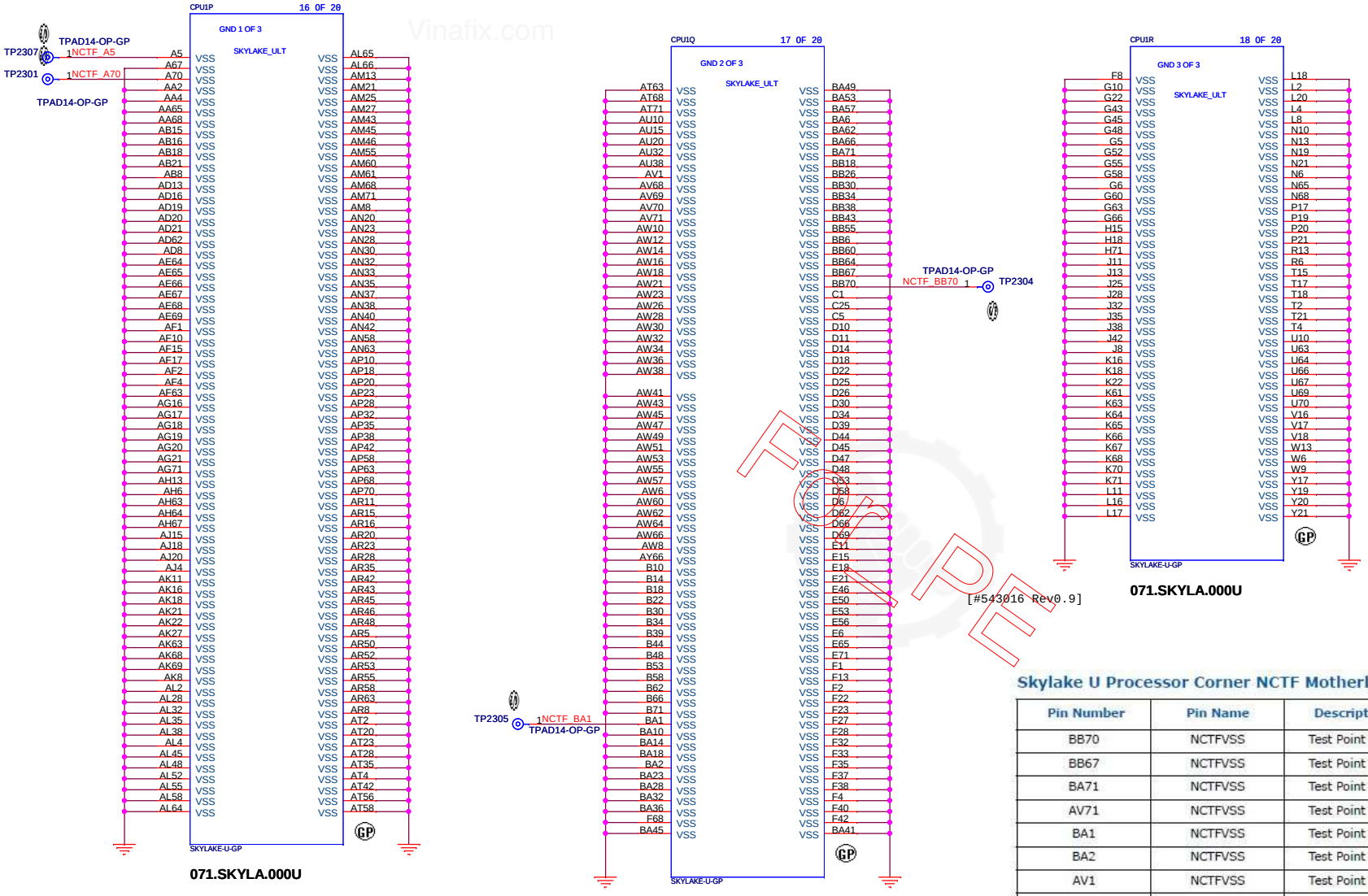
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(RSVD)***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 22 of 105

Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 23 of 105

Main Func = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X01 (SB)	100.0K	28.0K	2.75V
X02 (SC)	100.0K	33.0K	2.48V
X03(SD)	100.0K	47.0K	2.24V
A00 (I)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO97)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Vega_SKL_UMA	100.0K	10.0K(64.1002% EDI)	3.0V
Vega_SKL_DIS	100.0K	22.1K(64.2712% EDI)	2.791V
Turis_SKL_UMA	100.0K	32.4K(64.3242% EDI)	2.491V
Turis_SKL_DIS	100.0K	47.9K(64.2995% EDI)	2.201V
Vega_SKL_DIS	100.0K	64.9K(64.6457% EDI)	2.001V
Vega_KBL_DIS	100.0K	93.1K(64.5312% EDI)	1.791V
Turis_SKL_DIS	100.0K	128K(64.7281% EDI)	1.495V
Turis_KBL_DIS	100.0K	203K(64.7087% EDI)	1.095V

Layout Note:
Need very close to EC

Need very close to EC

Layout Note:
Need very close to EC

Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

ALL_SYS_PWRGD asser't, delay 10ms; RESET_OUT# assert

EC LCD test

EVT1 2014/10/20

Power Switch Logic(PSL)

EC_GPIO47 High Active

MEC1404

071.01404.000E

MEC1404-NU-GP

082.30003.0201

83.R2004.G8F

83.R2004.G8F

83.R2004.G8F

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

Q2412 and Q2413 merge

75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.J31

EC_DEBUG

20.K0691.006

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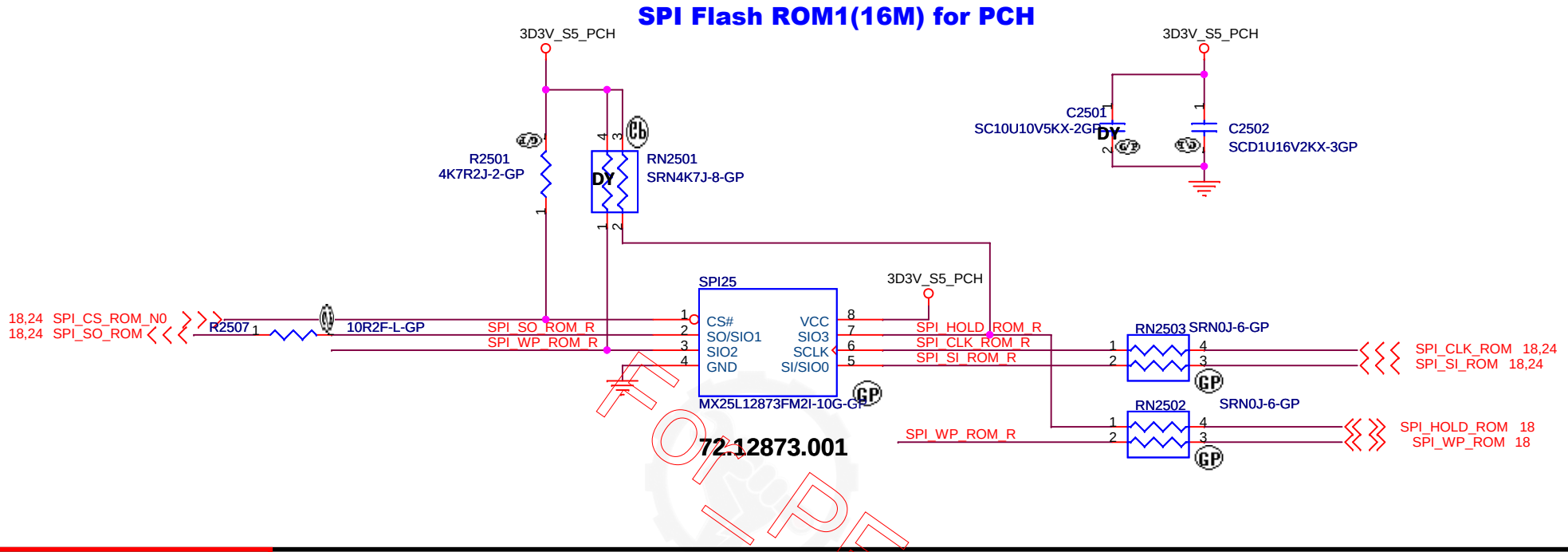
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC SMSC 1404

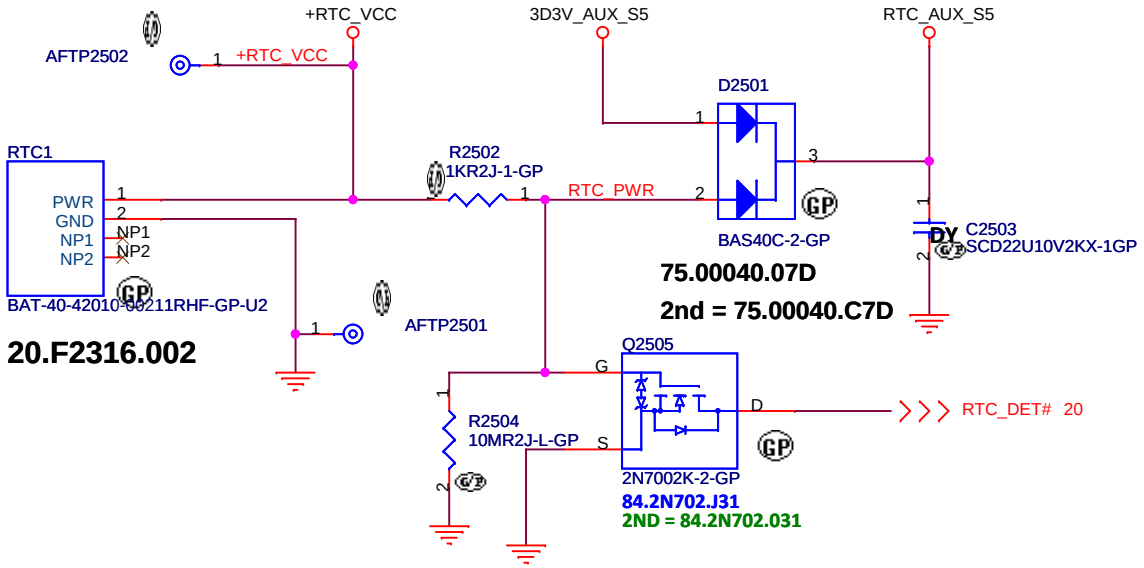
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 24 of 105

Main Func = SPI Flash



Main Func = RTC



<Core Design>

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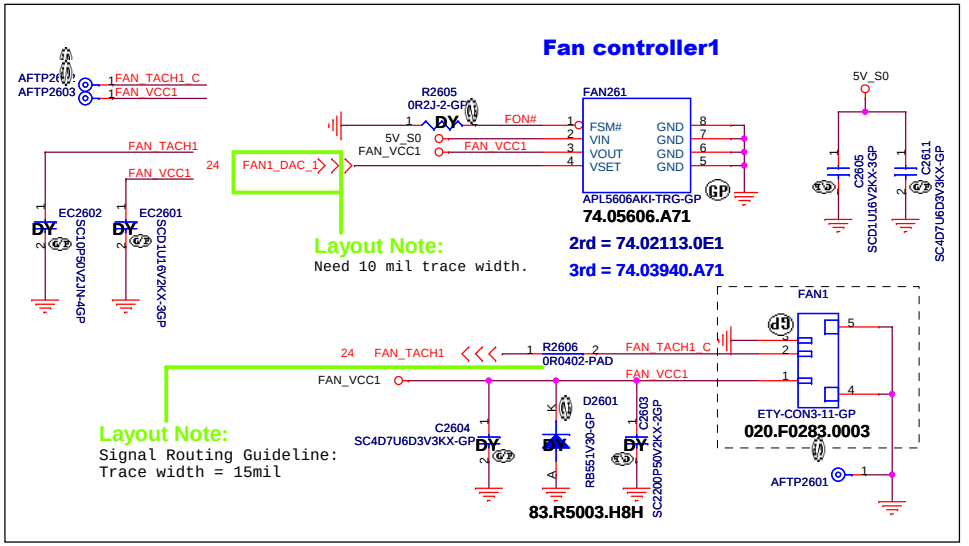
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

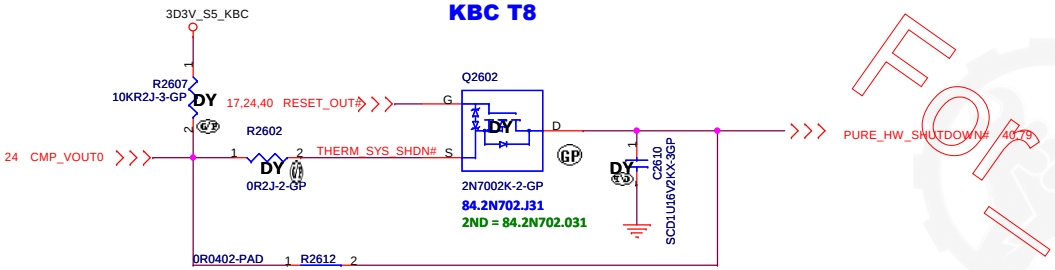
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

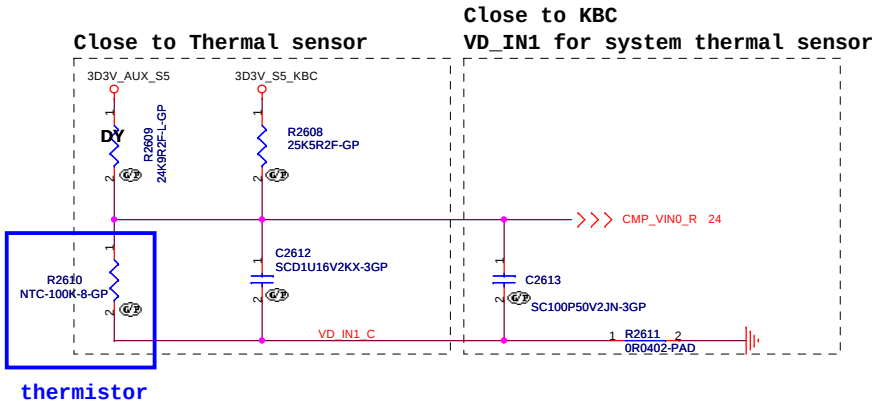
Date: Monday, June 27, 2016 Sheet 25 of 105

Main Func = Thermal Sensor



change the fan define & connect P/N 020.F0283.0003 by Andy 1/27





<Core Design>

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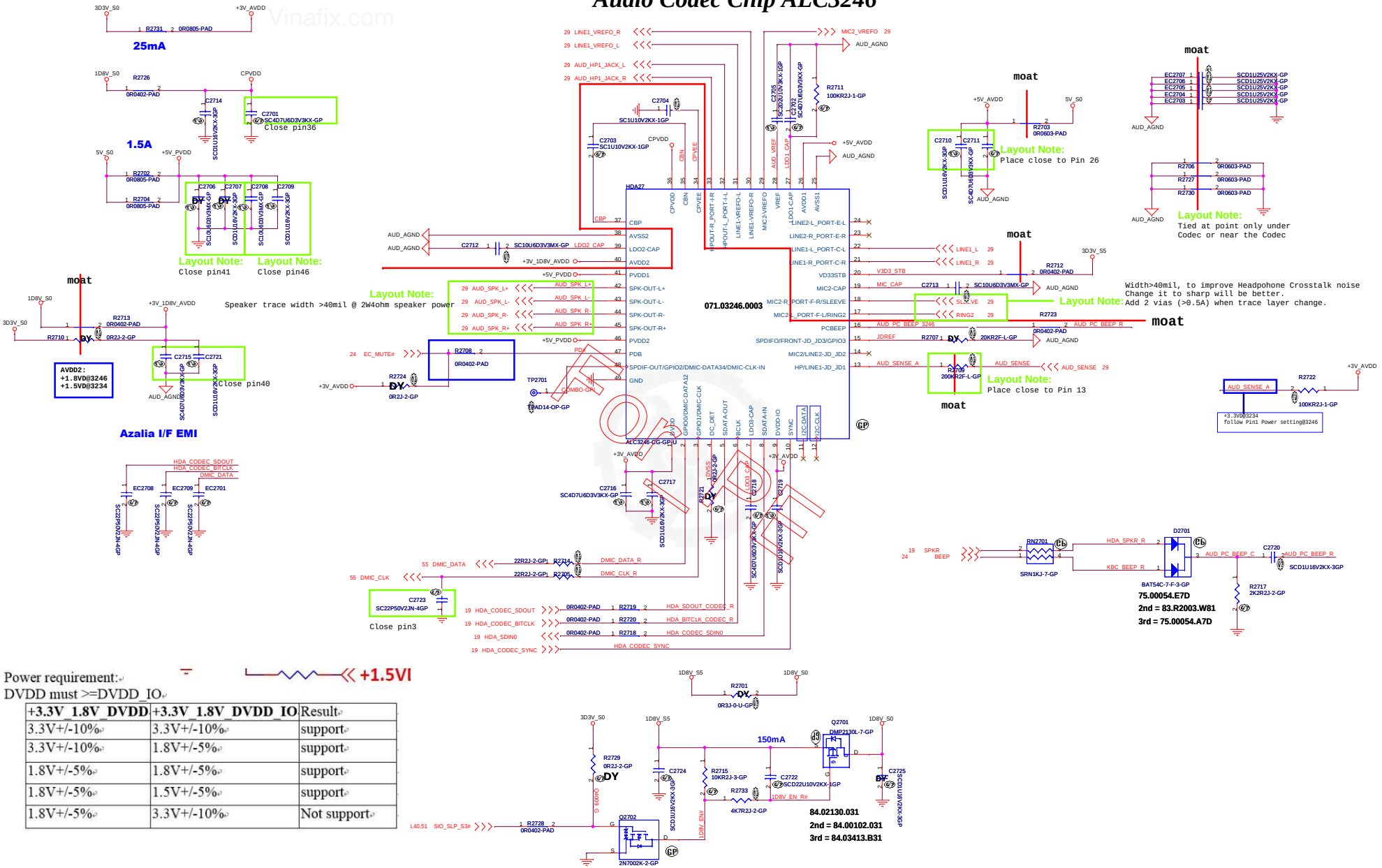
Title	THERMAL NCT7718W/Fan	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 26 of 105	

Main Func = Audio

Audio Codec Chip ALC3246



Power requirement:
DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

<Core Design>

Wistron Corporation
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Title: Audio Codec ALC3246

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 27 of 109

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<Core Design>

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Title

(Reserved)

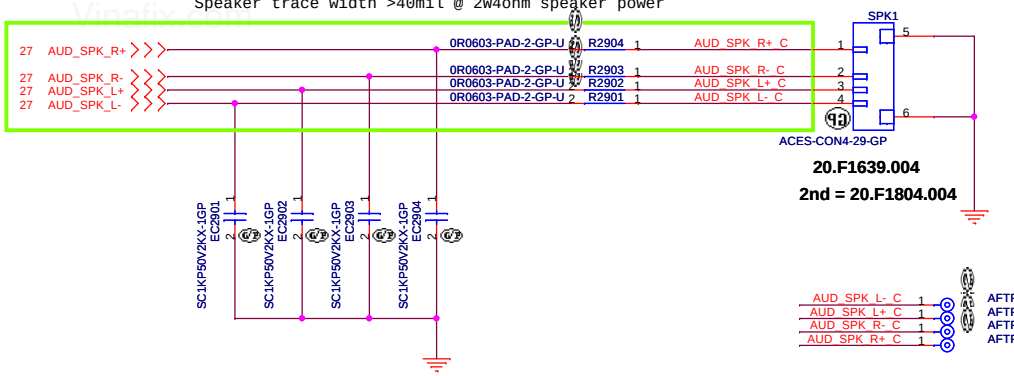
Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 28 of 105

Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

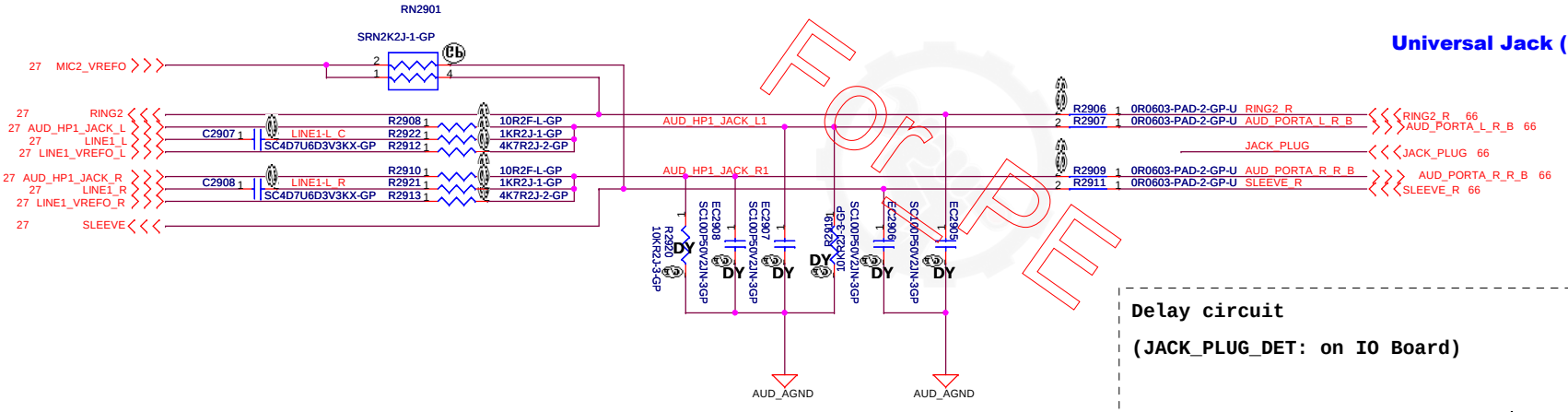


20.F1639.004

2nd = 20.F1804.004

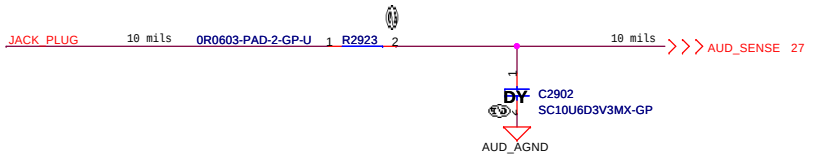
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Delay circuit

(JACK_PLUG_DET: on IO Board)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 29 of 105

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

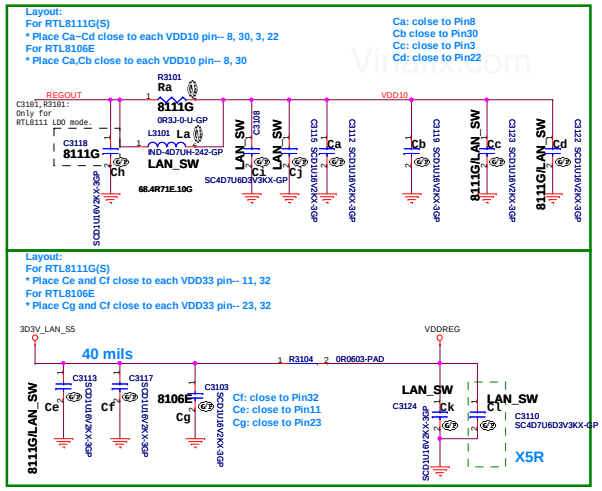
(Reserved)

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

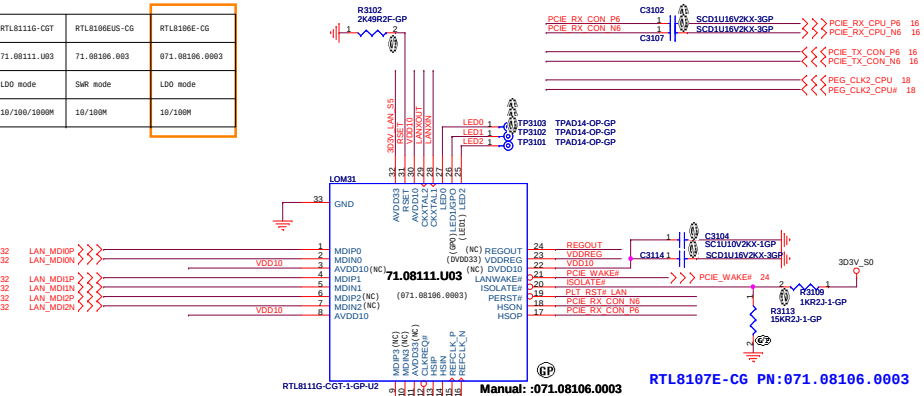
Date: Thursday, June 16, 2016 Sheet 30 of 105

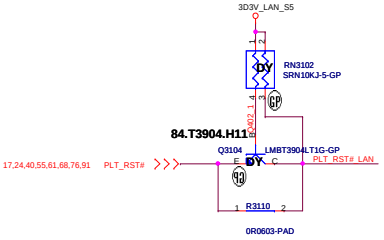
Main Func = LAN

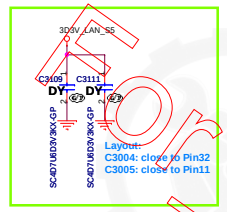
LAN CHIP (10/100/1000M & 10/100M co-lay)



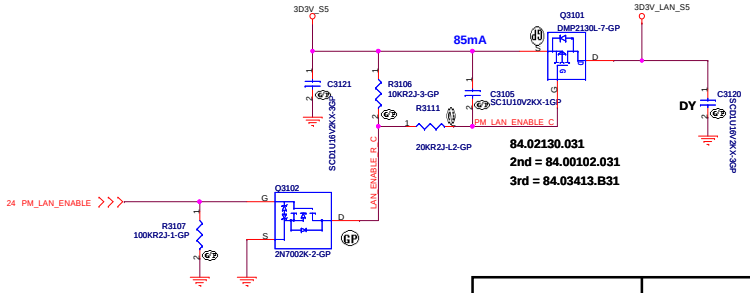
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

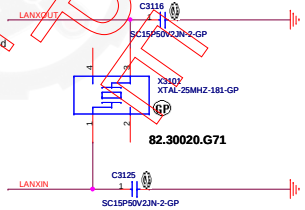


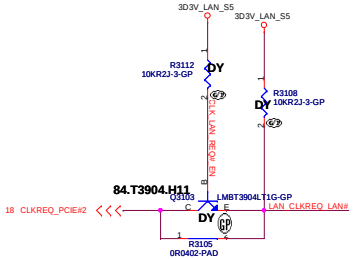




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	BOM Option	1.0V Source	Ra	Ch	Cc	Cd	Ce	La	Ci	Cj	Ck	Cl	Cg
RTL8111G-CGT (71.08111.U03)	8111G	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	LAN_SW	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	8106E	LDO	X	X	X	X	X	X	X	X	X	X	O

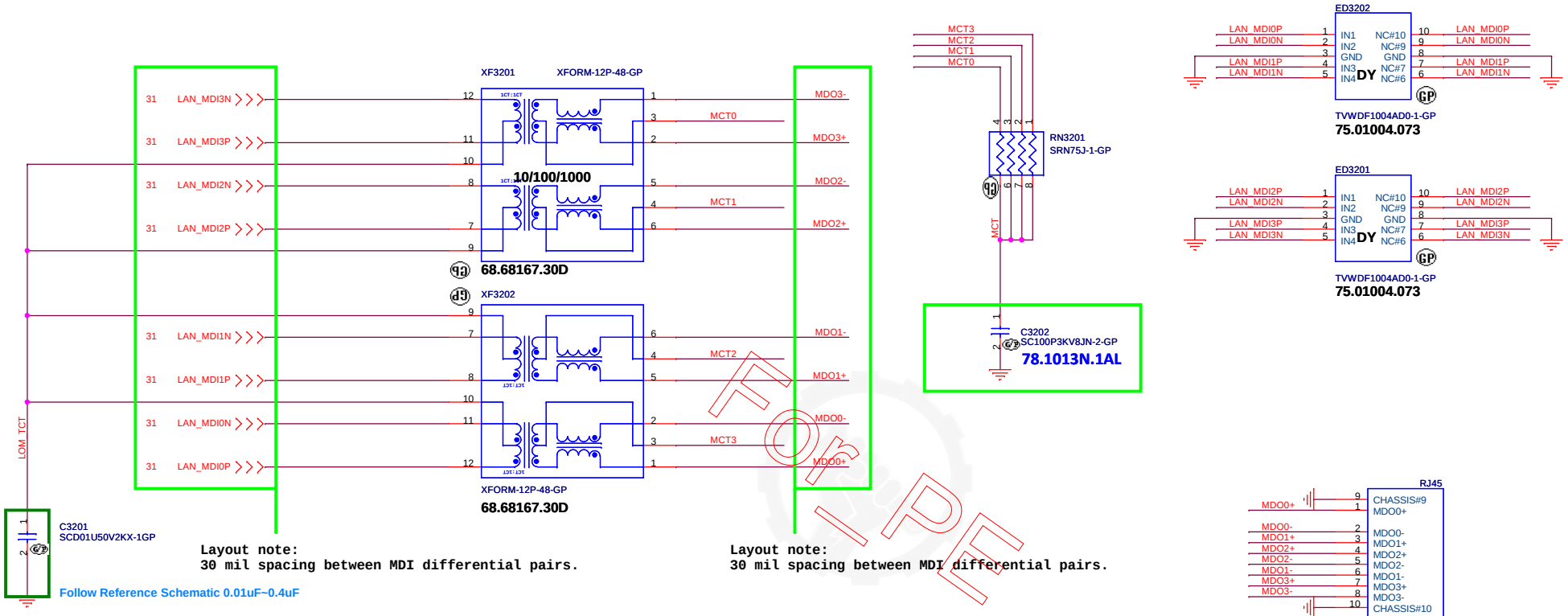
Title: LAN RTL8106

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

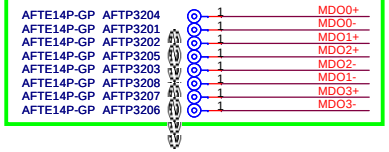
Date: Monday, June 27, 2016 | Sheet 31 of 105

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)



Layout:
Place near RJ45



<Core Design>

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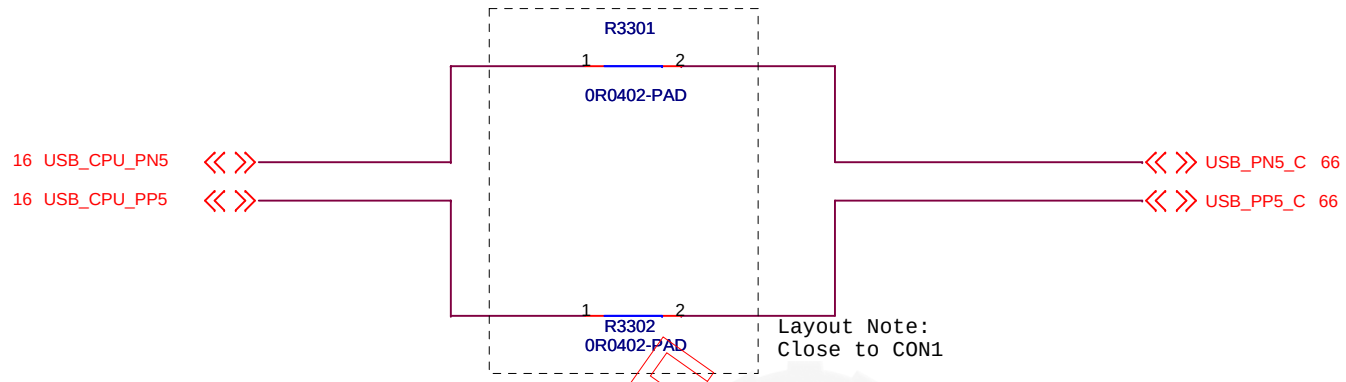
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 32 of 105

Main Func = Card Reader



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5170

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 33 of 105

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<Core Design>

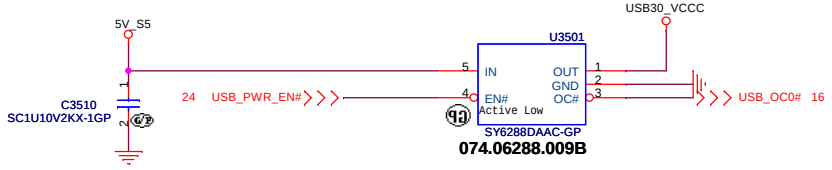
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

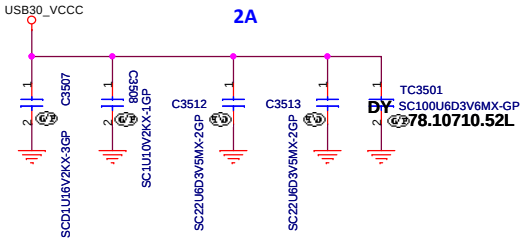
Date: Thursday, June 16, 2016 Sheet 34 of 105

Main Func = USB3.0 Port1

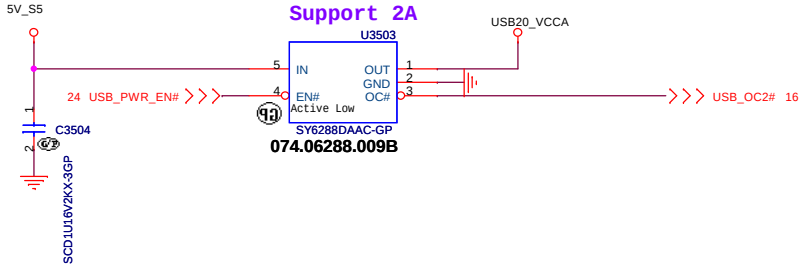


USB3.0 Port1

Layout Note: Close USB1

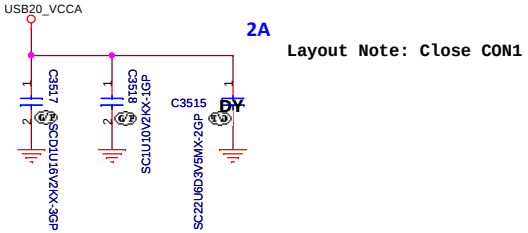


Main Func = USB2.0 Port3

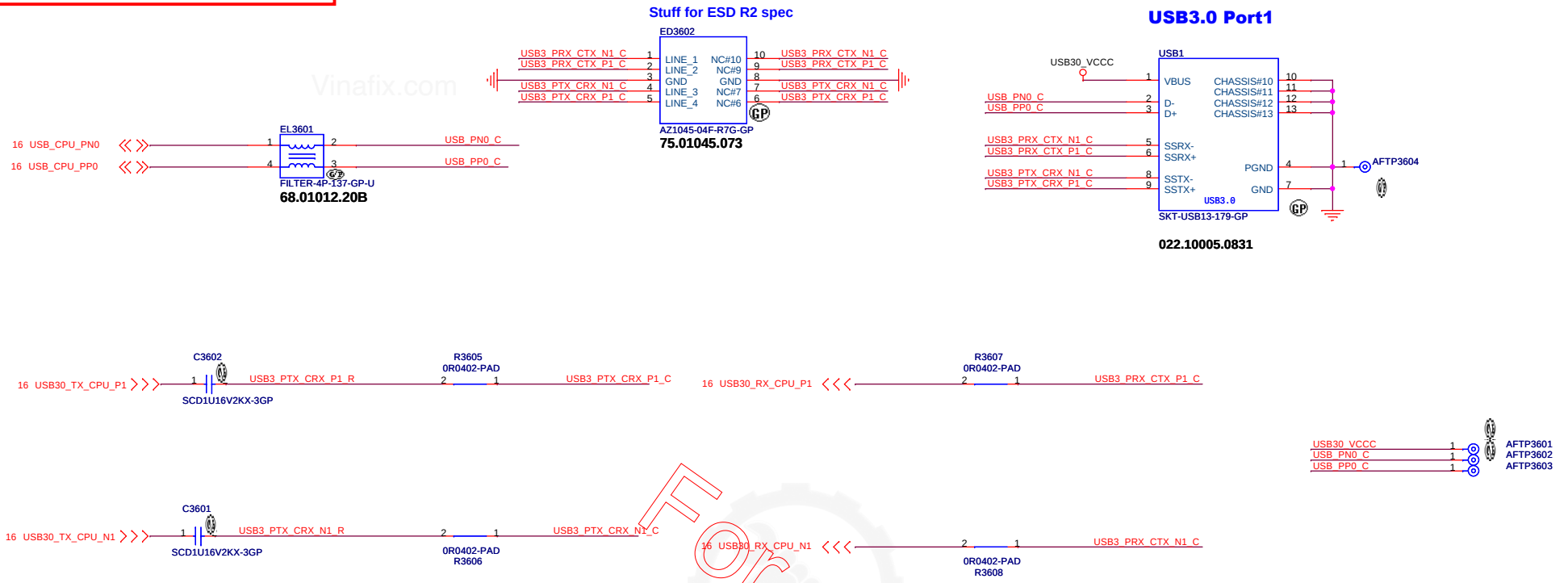


USB2.0 Port3 (IO Board)

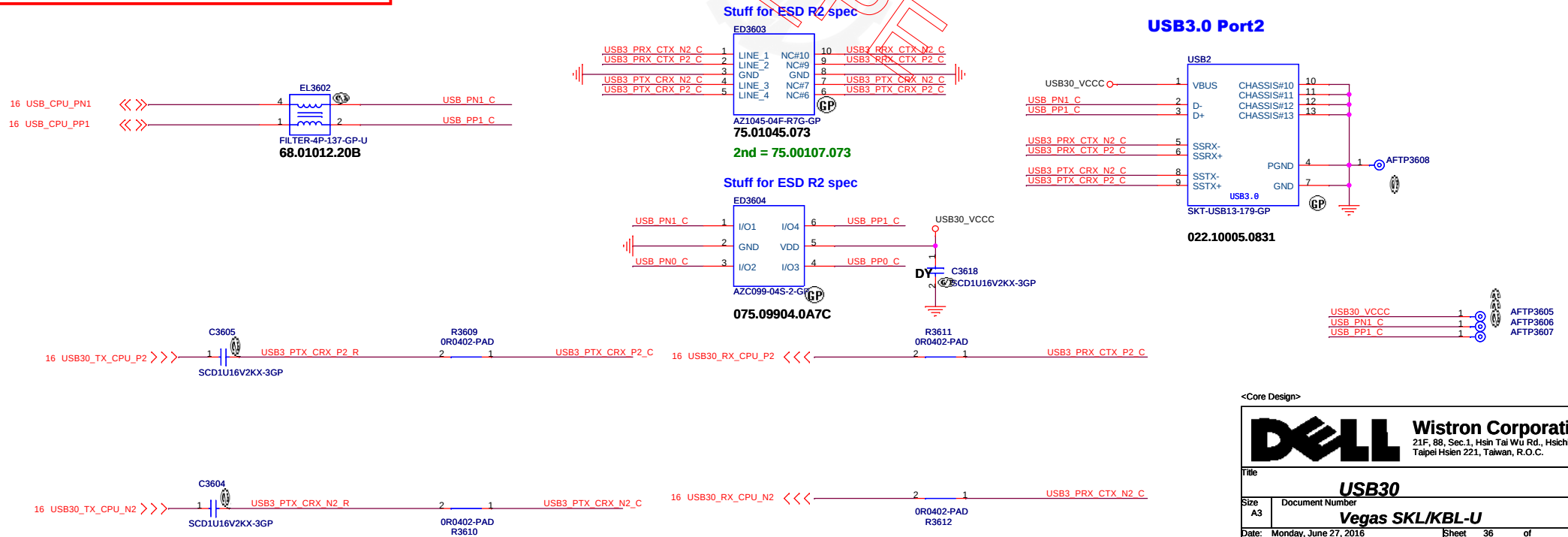
Layout Note: Close CON1



Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
A3	Vegas SKL/KBL-U	A00

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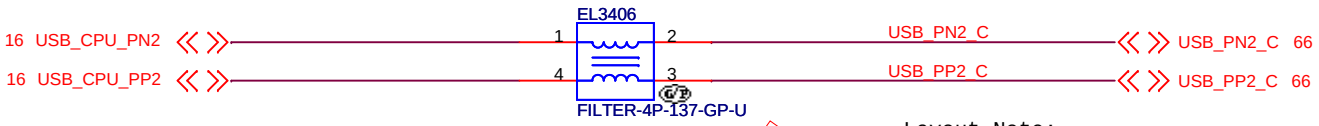
Main Func = USB2.0 Port3

USB port 3 (USB2.0 only) CMC

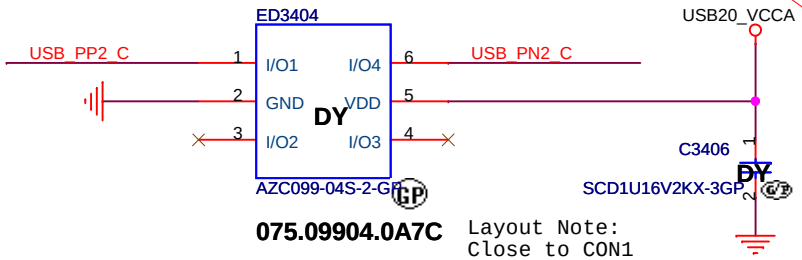


68.01012.20B

Layout Note:
Close to CON1

USB ESD Diode

Stuff for ESD R2 spec



075.09904.0A7C

Layout Note:
Close to CON1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB20*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Monday, June 27, 2016 Sheet 37 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

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(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

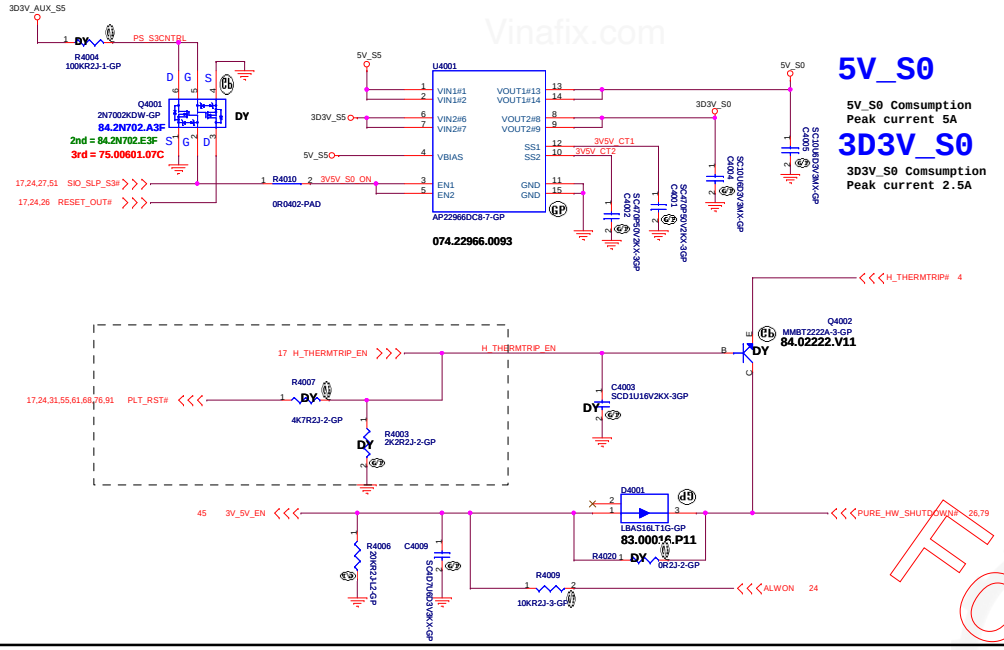
(Reserved)

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

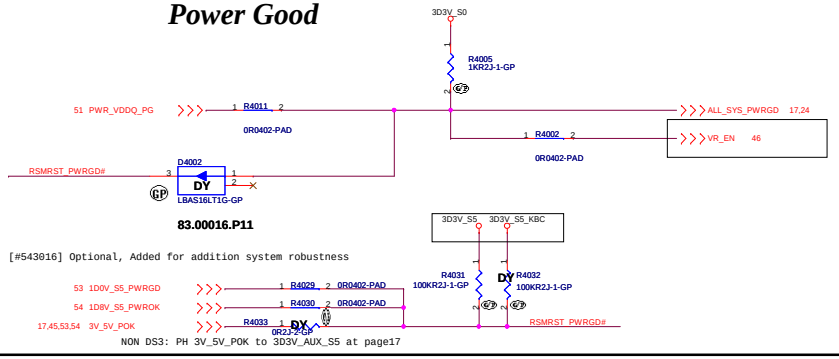
Date: Thursday, June 16, 2016 Sheet 39 of 105

Main Func = Power Plane & Sequence

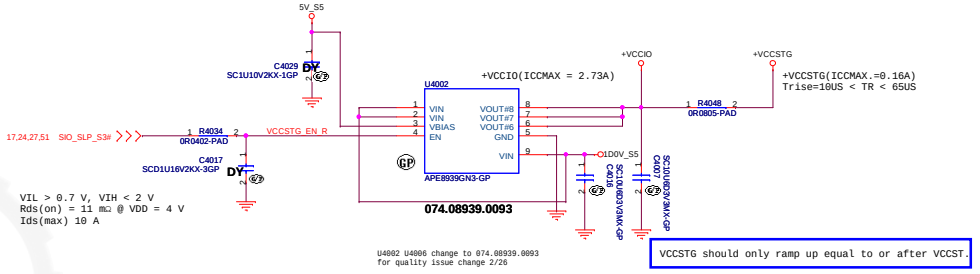
ROSA Run Power



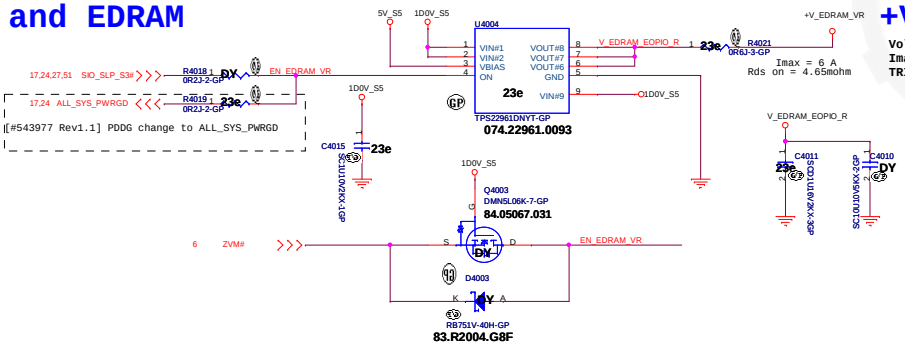
Power Good



VCCSTG and VCCIO



EOPIO and EDRAM



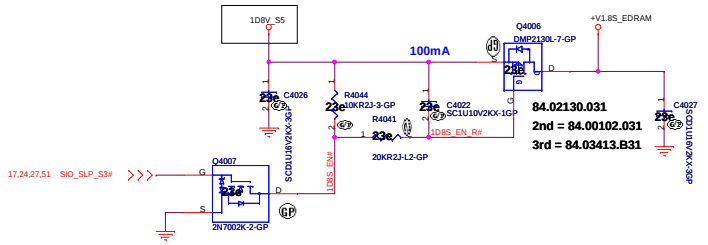
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

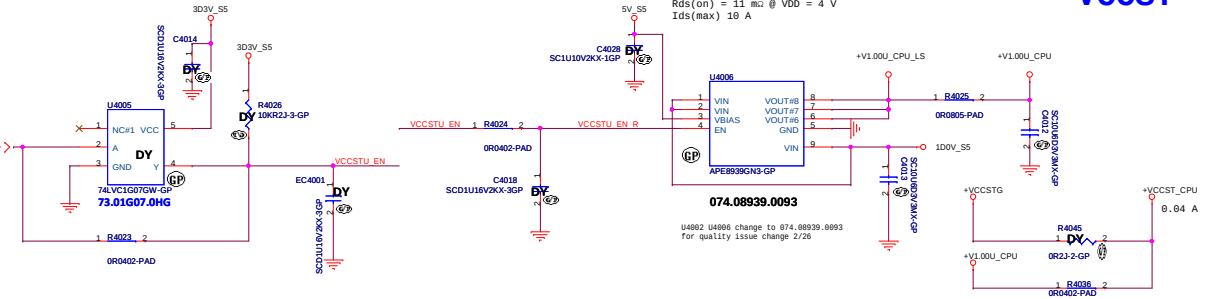
V1.8S



MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



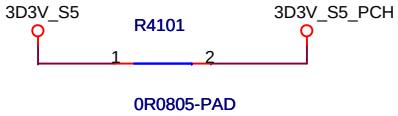
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 40 of 105

Main Func = Power & Sequence



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Connected_Standby(1/2)+DS3***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 41 of 105

(Blanking)

<Core Design>

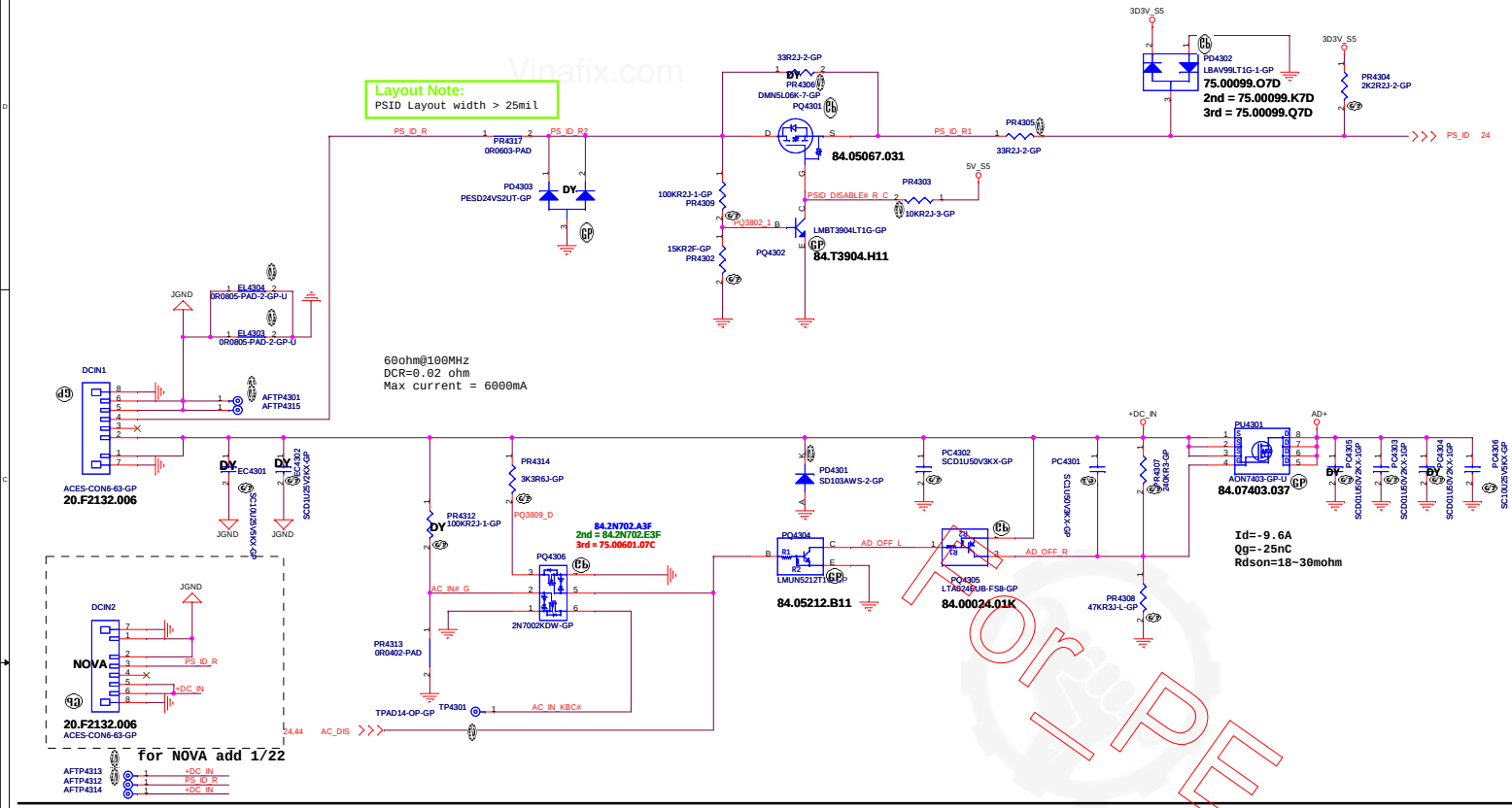
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

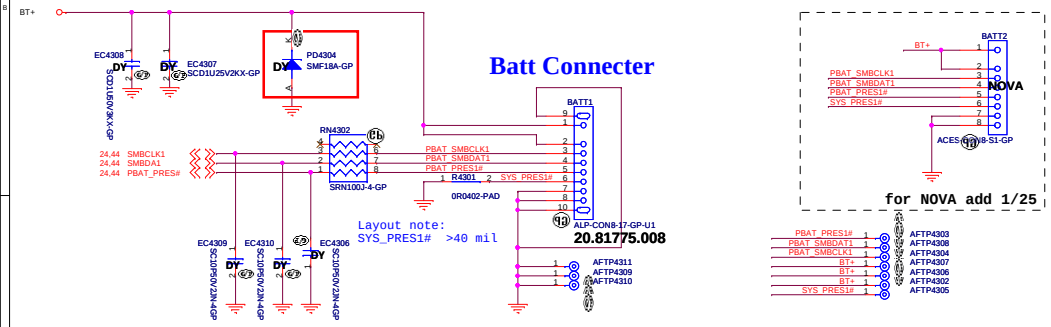
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

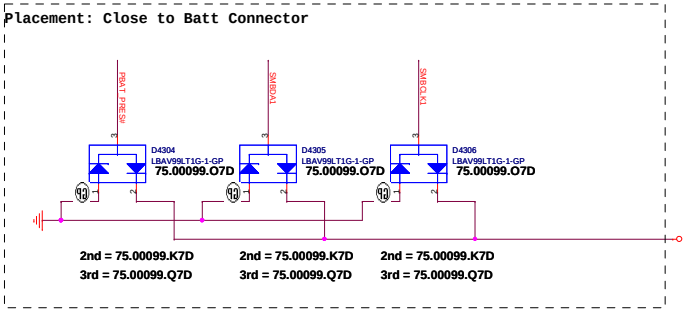
Date: Thursday, June 16, 2016 Sheet 42 of 105

Main Func = ADT Input

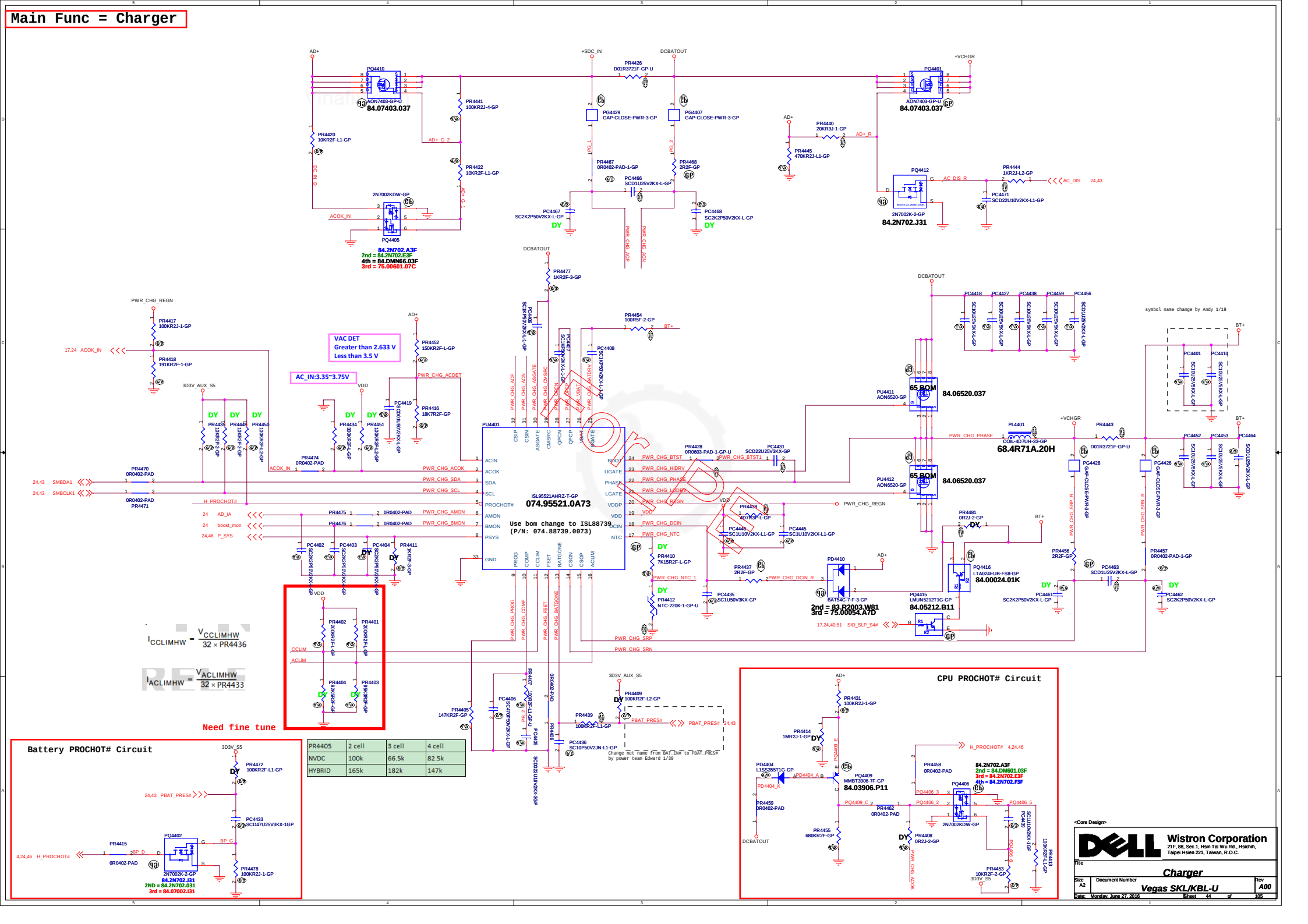


Main Func = M-BAT Input

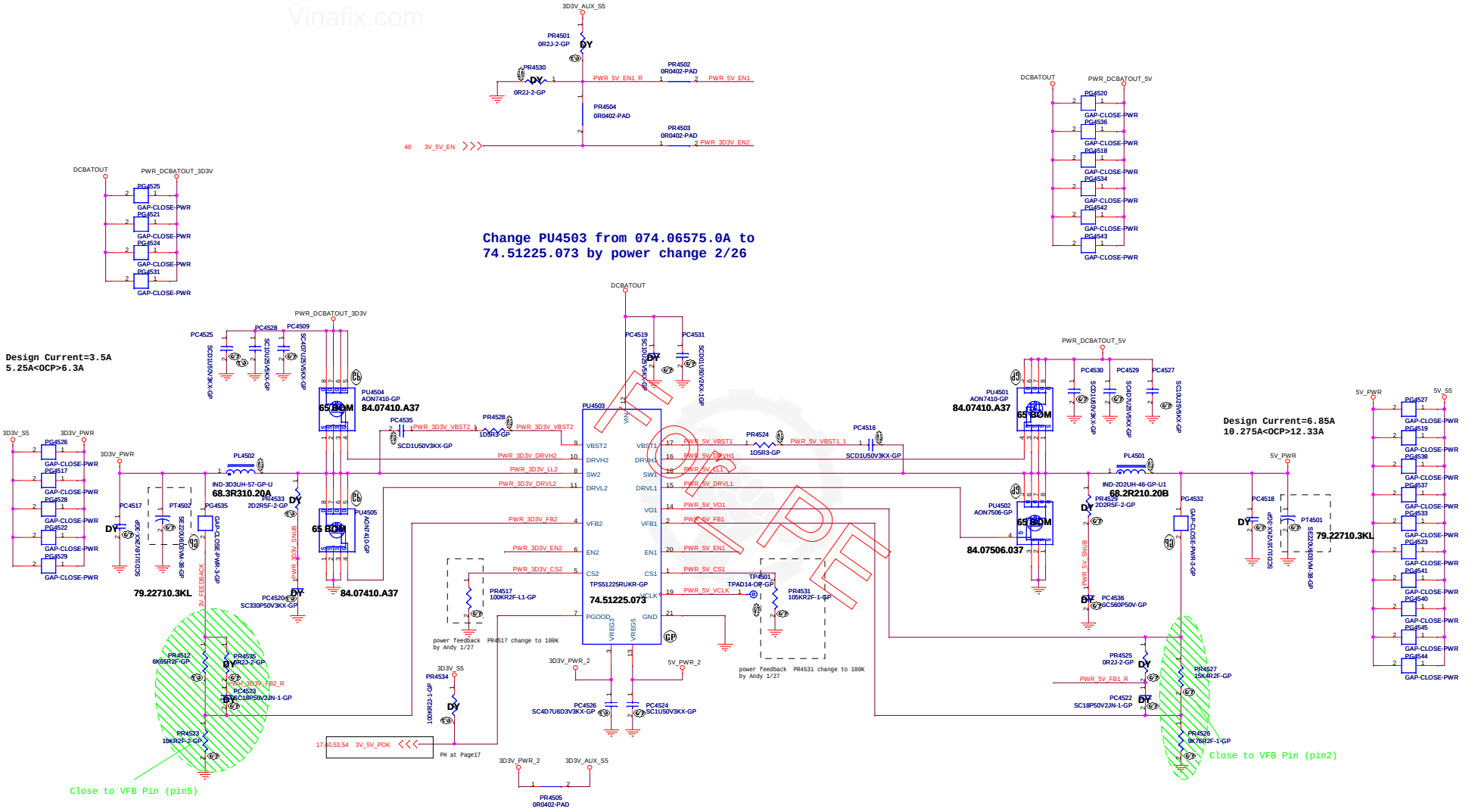




Main Func = Charger



Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-3D3V&5V

Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

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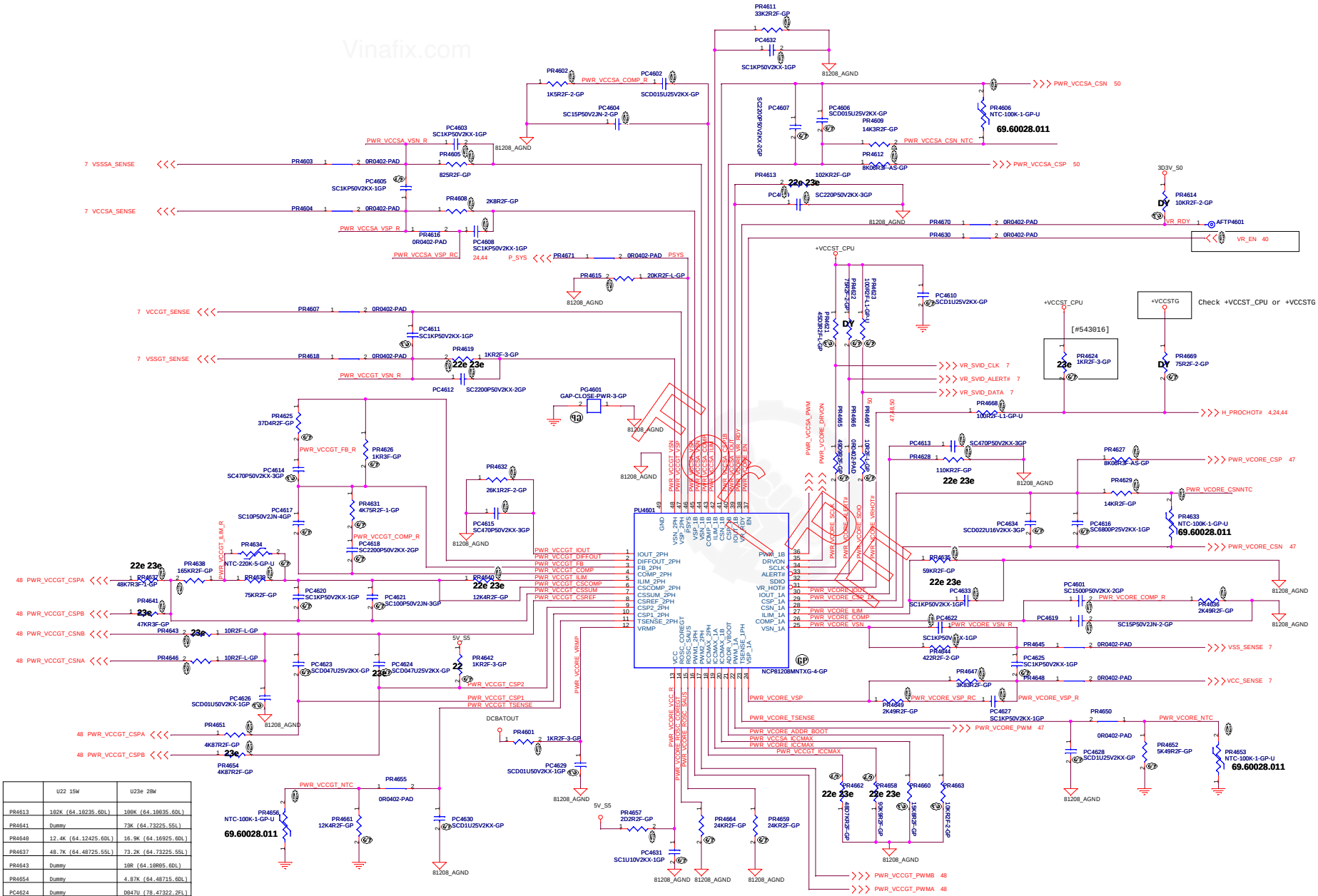
Main Func = CPU_CORE



	U22 15W	U23e 28W
PR4613	102K (64.10235.6DL)	100K (64.10035.6DL)
PR4641	Dummy	73K (64.73225.55L)
PR4640	12.4K (64.12425.6DL)	16.9K (64.16925.6DL)
PR4637	48.7K (64.48725.55L)	73.2K (64.73225.55L)
PR4643	Dummy	10R (64.10R05.6DL)
PR4654	Dummy	4.87K (64.48715.6DL)
PC4624	Dummy	D047U (78.47322.2FL)
PR4642	1K (64.10015.6DL)	Dummy
PR4662	48.7K (64.48725.6DL)	100K (64.10035.6DL)

<Core Design>

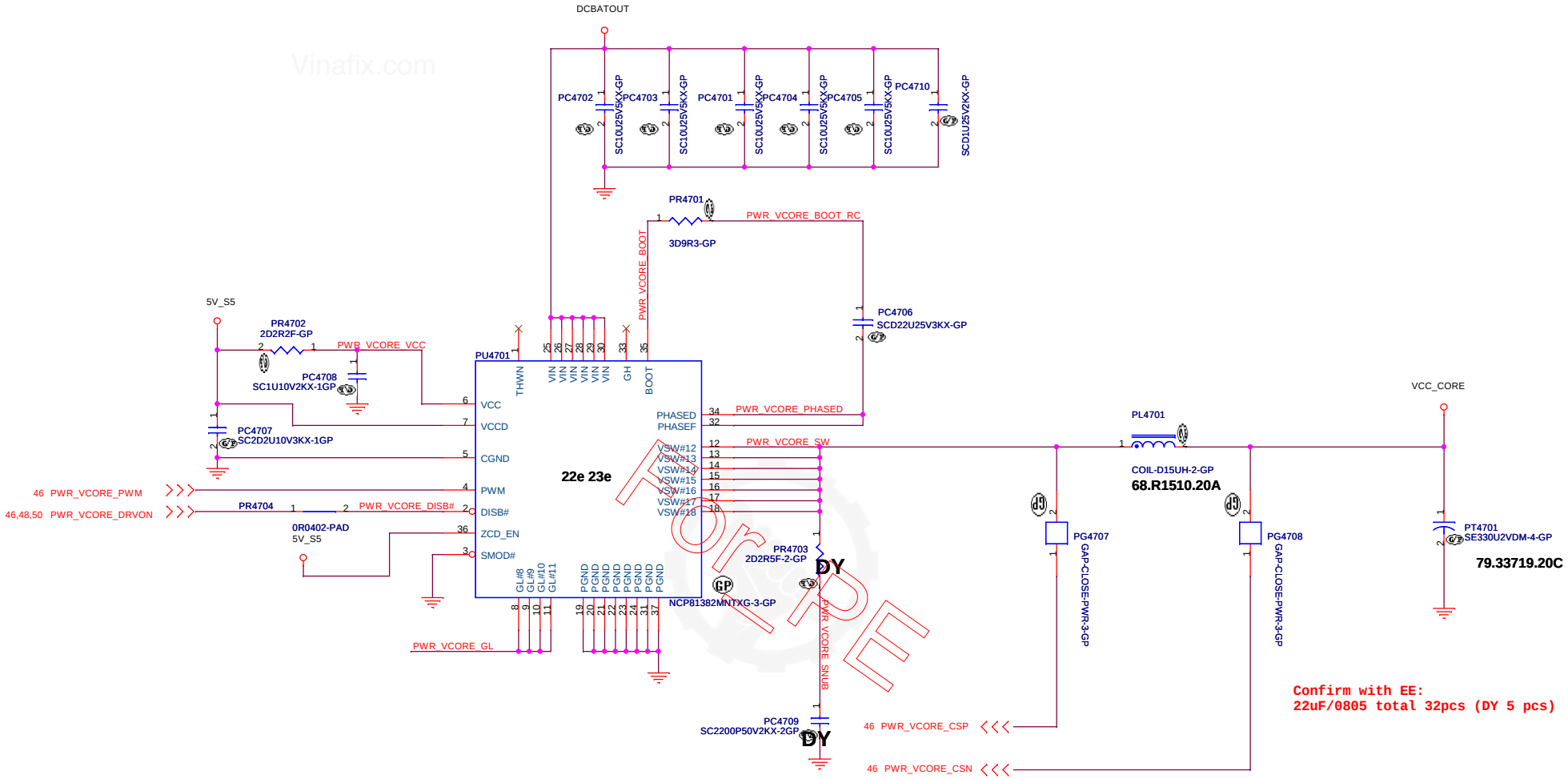
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 46 of 105

Main Func = CPU_CORE



<Core Design>

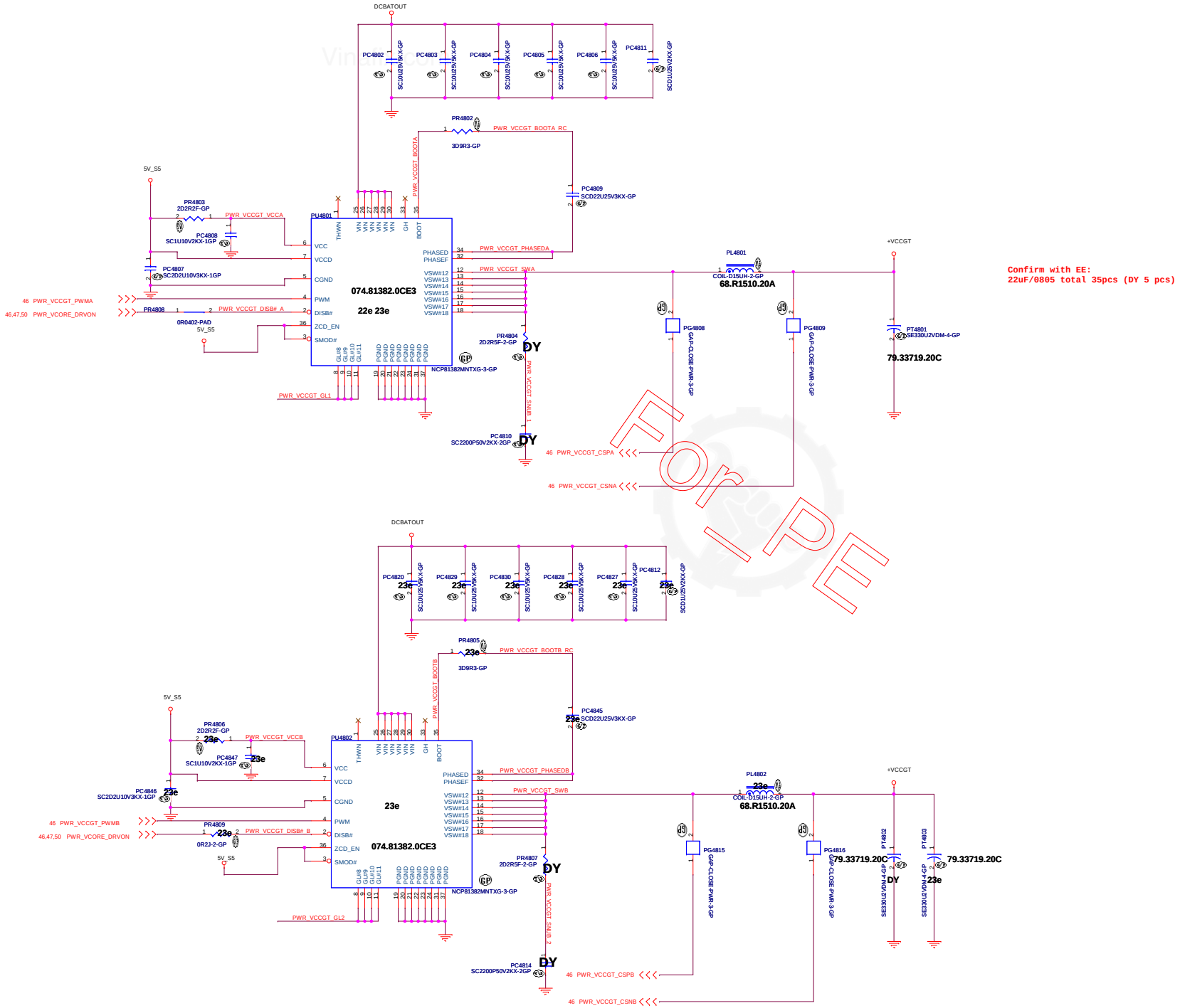
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCORE(2/3)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 47 of 105

Main Func = CPU_CORE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 48 of 105

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<Core Design>

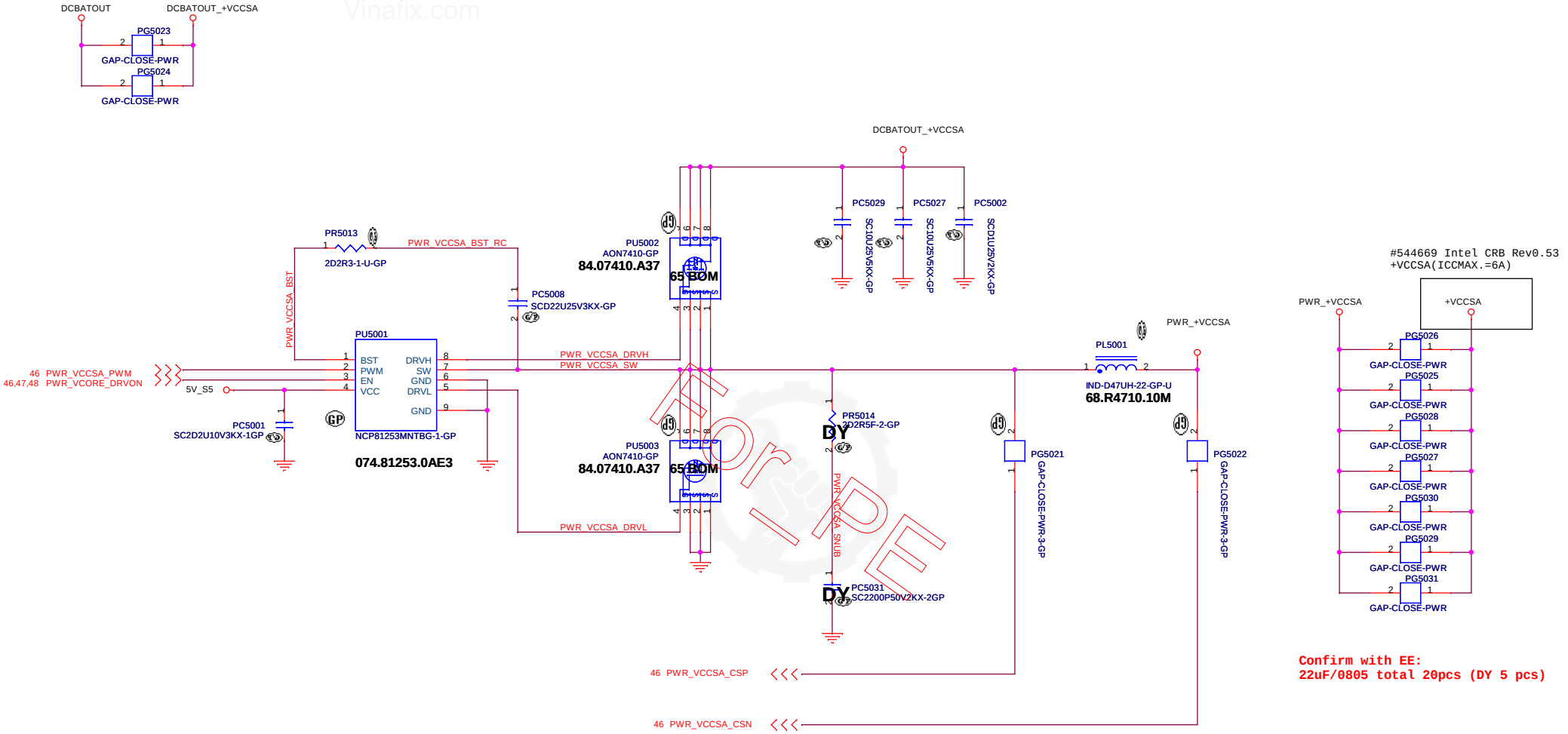
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

Size: A4 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 49 of 105

Main Func = CPU_CORE



#544669 Intel CRB Rev0.53
+VCCSA(ICCMAX.=6A)

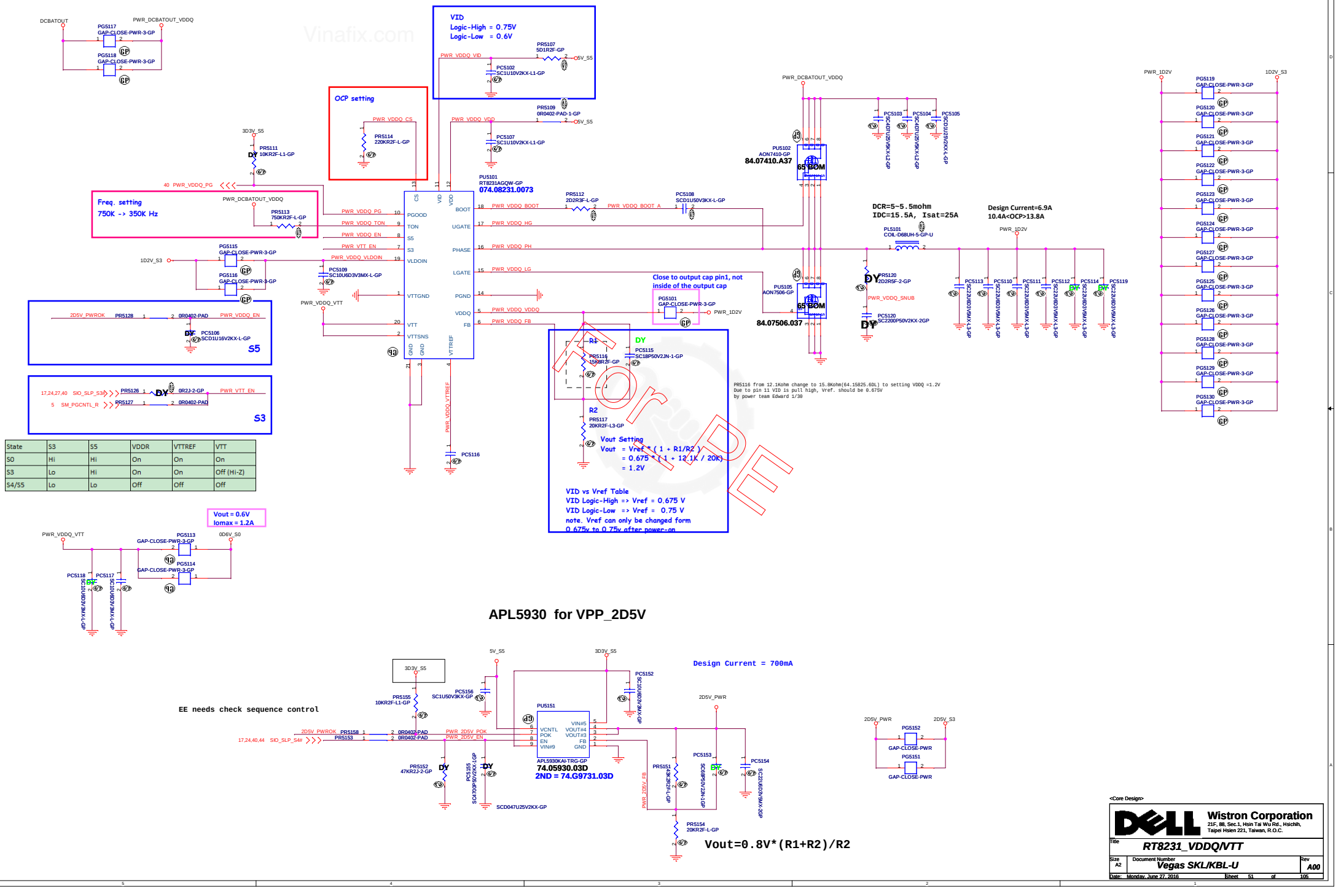
Confirm with EE:
22uF/0805 total 20pcs (DY 5 pcs)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81253MN_CPU_VCCSA	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1p2v& 2D5V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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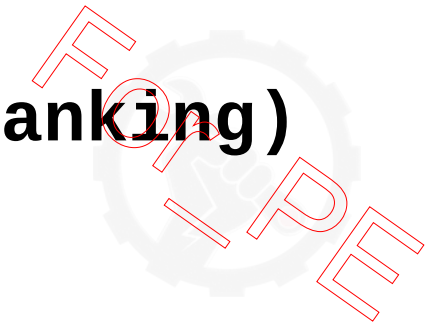
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_VDDQ/VTT

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 51 of 105

(Blanking)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

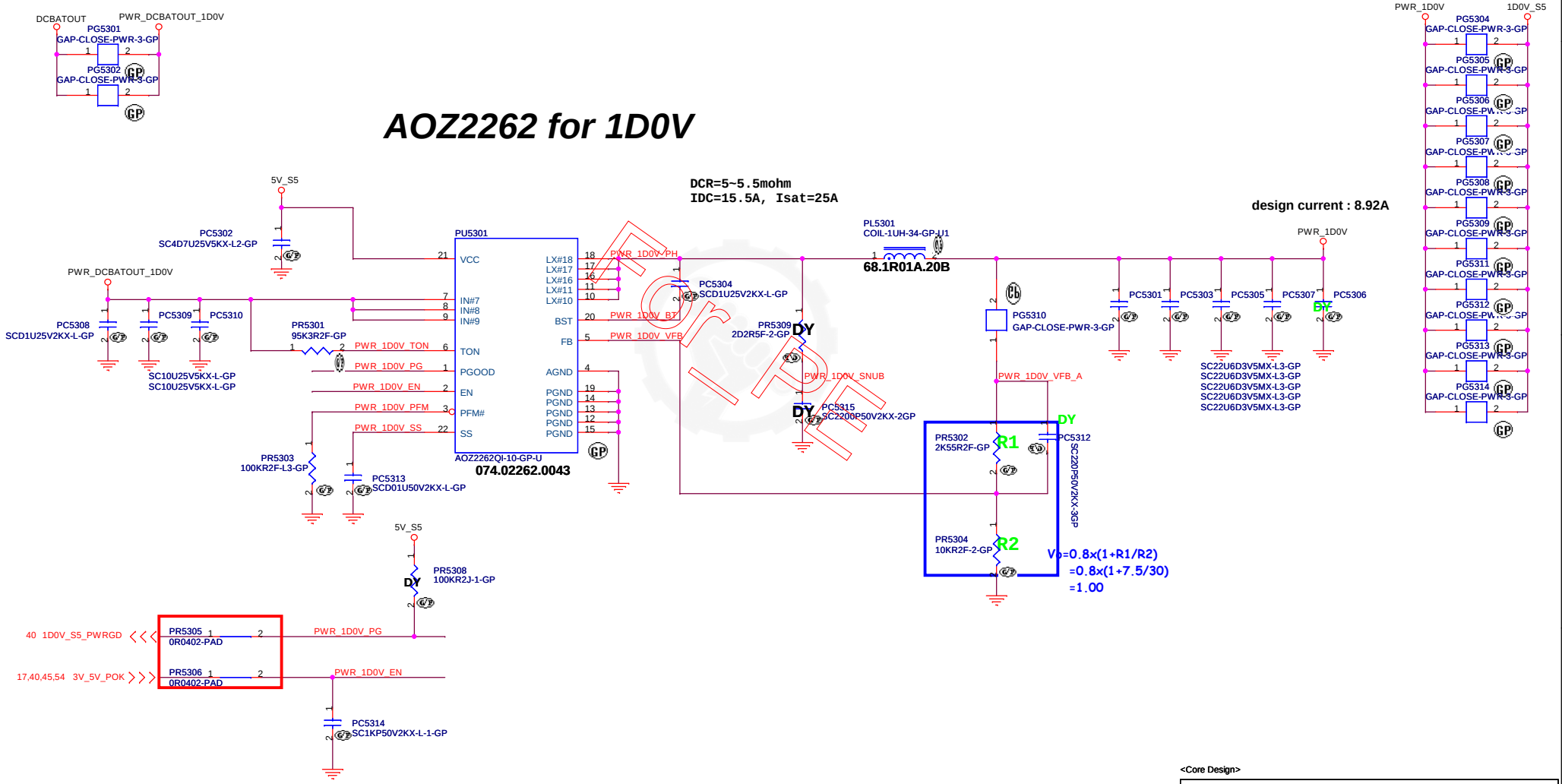
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 52 of 105

SSID = PWR.Plane.Regulator_1p0v

AOZ2262 for 1D0V



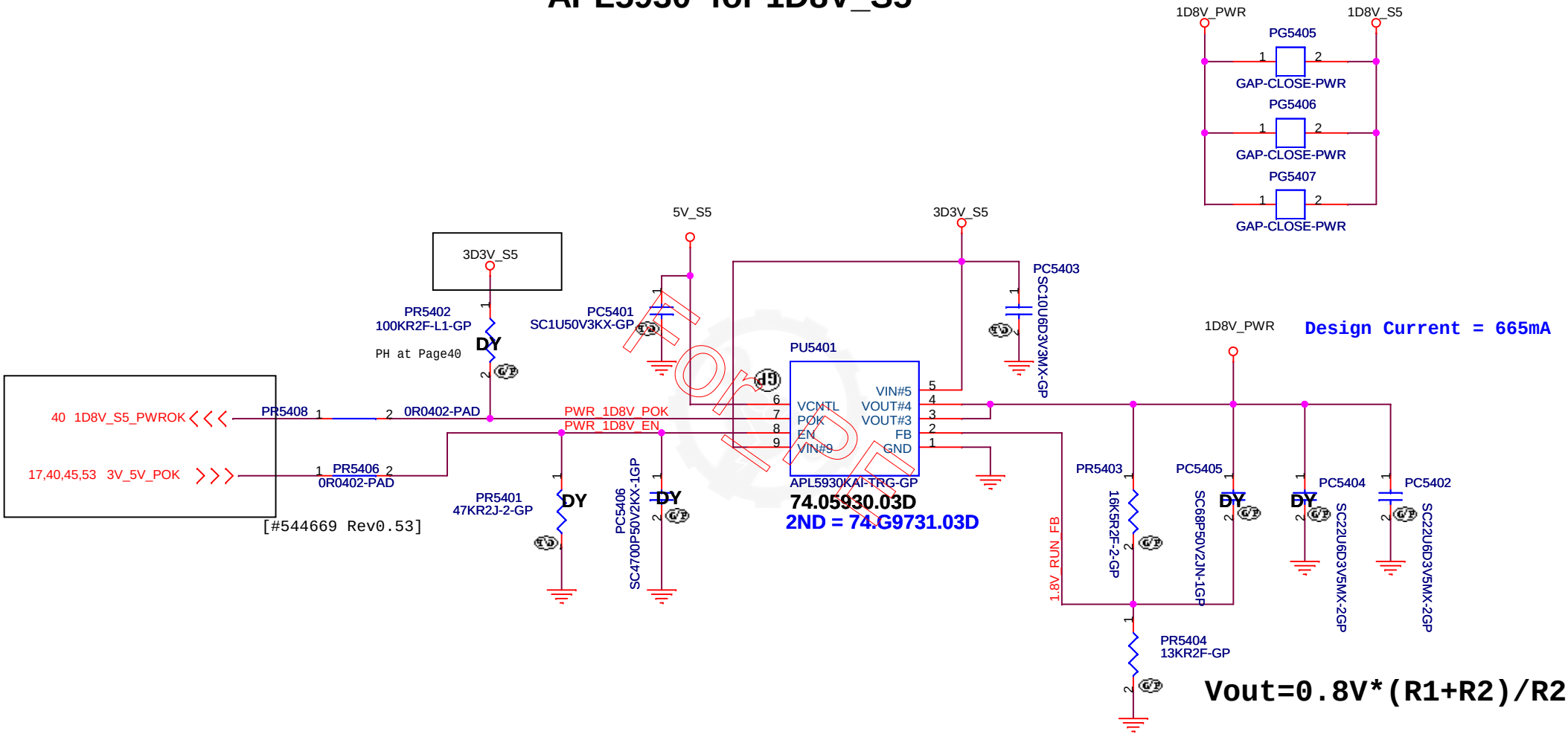
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AOZ2262QI_1D0V	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 53 of 105	

Main Func = 1D8V

APL5930 for 1D8V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO-V1D5V&V1D8V*		
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Monday, June 27, 2016	Sheet 54 of 105	

Main Func = LCD

LCD1
IPEX-CON40-3-GP
20.F1407.040
Trace width = 80mil
Layout Note:
Colse to LCD1.

LCD
Camera
Touch Panel

INVERTER POWER

EE note: Never change R5211 to short pad after MP

R5523 0R5J-5-GP
R5518 100R2J-2-GP
R5501 0R0402-PAD
add for camera detect pin 1/25
F5503 POLYSW-1D1A24V-GP-U 800mA
69.50007.A31
C5535 SCD1U50V3KX-GP
C5515 SC10U6D3V2KX-4GP
R5521 10KR2J-3-GP
R5525 100R2J-2-GP
R5526 0R2J-2-GP
For ESD
For AUDIO Grade B or C selection.

PU/PD FOR AUX CHANNEL

SKL PDG (#543016):
Recommends having a pull-up resistor of 100 kΩ for AUXN
and a pull-down resistor of 100 kΩ for AUXP
between the AC capacitor and the connector,
to assist source detection by the sink device.

R5528 100KR2J-1-GP
R5529 100KR2J-1-GP

RN502 SRN100KJ-5-GP
RN503 SRN100J-4-GP
R5524 0R2J-2-GP
D5503 BAT54C-7-F-3-GP
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
EC (BIST MODE)
R5531 0R0402-PAD
EC5504 SC22P50V2JN-4GP
R5527 0R0603-PAD
R5522 0R3J10-1GP
R5520 0R3J-0-U-GP
F5502 POLYSW-1D1A24V-GP-U
69.50007.A31
C5533 SCD1U50V3KX-GP

Brightness
R5530 0R0402-PAD

EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCDVDD

D5502 BAT54C-7-F-3-GP
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
R5506 100KR2J-1-GP
U5501 RT9724GB-GP
74.09724.09F
C5505 SC4D7U6D3V3KX-GP
Layout Note:
Trace width = 80mil

Main Func = CAMERA

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201

R5532 0R5J-5-GP
EC5503 SC33P50V2JN-3GP
C5539 SC4D7U6D3V3KX-GP
R5533 0R0402-PAD
R5534 0R0402-PAD
R5502 0R0402-PAD
R5503 0R0402-PAD
EC5501 SC68P50V2CN-1GP
EC5502 SC68P50V2CN-1GP

Layout Note: Reduce the stubs.

Main Func = Touch panel

Touch Panel

R5537 0R0402-PAD
C5541 SC10P50V2JN-4GP
R5538 0R0402-PAD
C5540 SC10P50V2JN-4GP
R5535 0R0402-PAD
R5536 0R0402-PAD
ED5501 AZC099-04S-2-G
C5501 SCD1U16V2KX-3GP
075.09904.0A7C

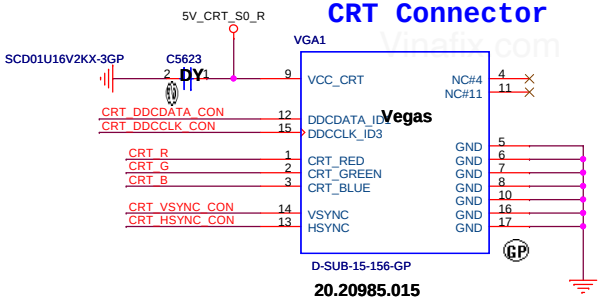
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: Custom
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Monday, June 27, 2016
Sheet 55 of 105

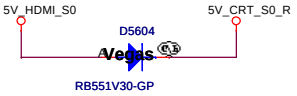
Main Func = CRT

CRT Connector

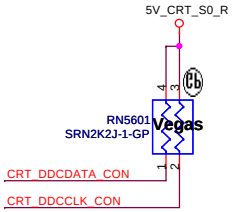


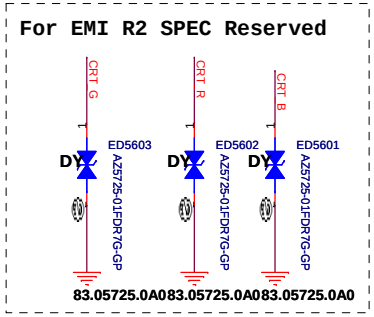
20.20985.015

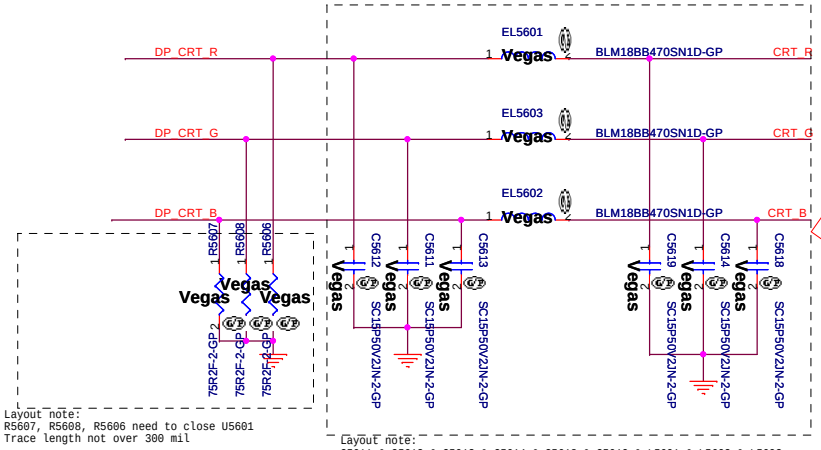
Change the VGA connect by Andy 1/14

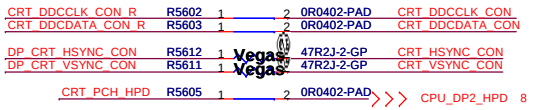


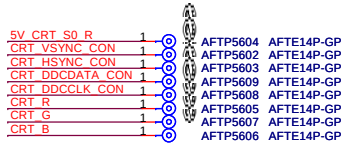
83.R5003.H8H

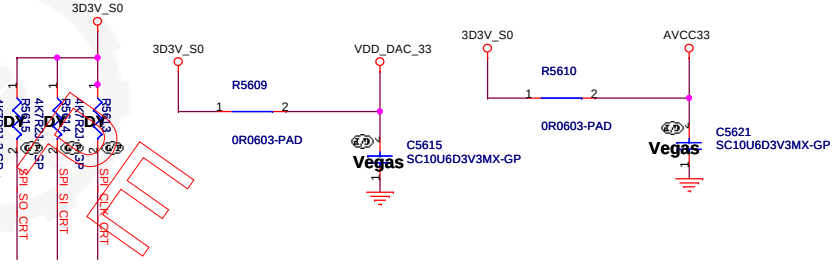


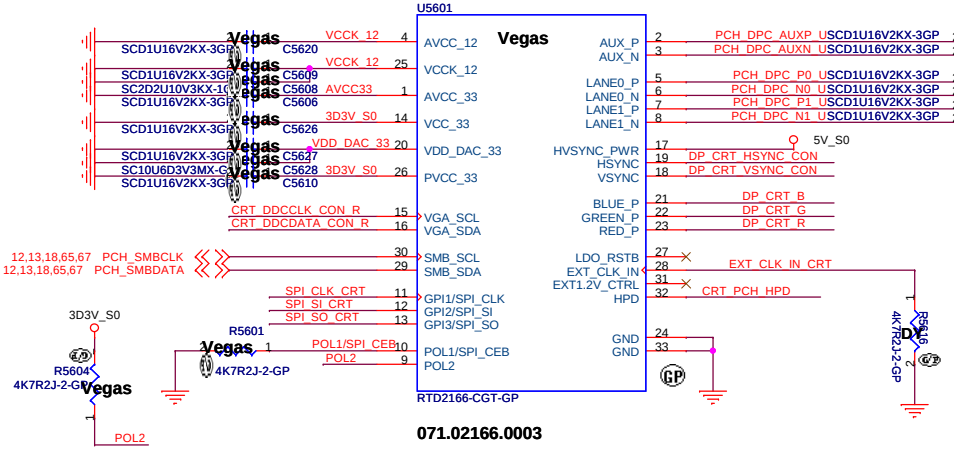




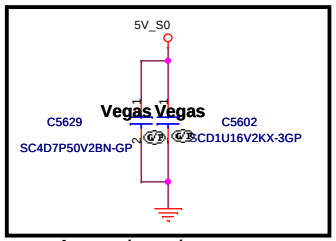




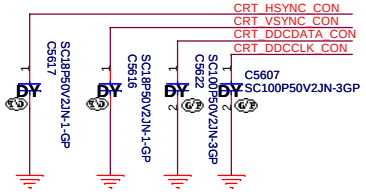




071.02166.0003



Layout note:
close to pin17



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 56 of 105	

Main Func = HDMI

8 HDMI_CLK#
8 HDMI_CLK
8 HDMI_DATA0#
8 HDMI_DATA0
8 HDMI_DATA1#
8 HDMI_DATA1
8 HDMI_DATA2#
8 HDMI_DATA2

C5701 C5704 SCD1U16V2KX-3GP → HDMI_CLK#_R / HDMI_CLK_R
C5705 C5703 SCD1U16V2KX-3GP → HDMI_DATA0#_R / HDMI_DATA0_R
C5707 C5706 SCD1U16V2KX-3GP → HDMI_DATA1#_R / HDMI_DATA1_R
C5708 C5709 SCD1U16V2KX-3GP → HDMI_DATA2#_R / HDMI_DATA2_R

RN5703 SRN470J-3-GP
RN5701 SRN470J-3-GP

5V_S0
Q5701
R5719 100KR2J-1-GP
2N7002K-2-GP
HDMI_PLL_GND
R5707 0R2J-2-GP

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

ER5706 HDMI_CLK#_R → HDMI_CLK#_R_C
ER5714 HDMI_CLK_R → HDMI_CLK_R_C
R5702 150R2J-L1-GP-U
0R0402-PAD

ER5713 HDMI_DATA0#_R → HDMI_DATA0#_R_C
ER5715 HDMI_DATA0_R → HDMI_DATA0_R_C
R5701 150R2J-L1-GP-U
0R0402-PAD

R5717
ER5716 HDMI_DATA2_R → HDMI_DATA2_R_C
R5703 150R2J-L1-GP-U
0R0402-PAD

ER5705 HDMI_DATA1#_R → HDMI_DATA1#_R_C
ER5704 HDMI_DATA1_R → HDMI_DATA1_R_C
R5708 150R2J-L1-GP-U
0R0402-PAD

69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend

5V_S0 F5701 5V_HDMI_S0
POLYSW-1D1A6V-9-GP-U
R5718 0R3J-0-U-GP
69.48001.081
2ND = 69.50011.081
3RD = 69.50013.061

5V_S0
D5701 BAW56-9-GP
75.00056.07D
DDC_CLK_PH1
DDC_DATA_PH2

3D3V_S0
Q5702 2N7002KDW-GP
RN5702 SRN2K2J-1-GP
8 CPU_DP1_CTRL_CLK → DDC_CLK_HDMI
8 CPU_DP1_CTRL_DATA → DDC_DATA_HDMI

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

HDMI CONN

5V_HDMI_S0
C5702 SCD1U16V2KX-3GP

HDMI1
+5V_POWER
HDMI_DATA0_R_C
HDMI_DATA0#_R_C
HDMI_DATA1_R_C
HDMI_DATA1#_R_C
HDMI_DATA2_R_C
HDMI_DATA2#_R_C
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
HDMI_CLK_R_C
HDMI_CLK#_R_C
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL → DDC_CLK_HDMI
SDA → DDC_DATA_HDMI
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND GND GND GND
HDMI (A_Type)
SKT-HDMI23-168-GP

022.10025.0161

HPD_HDMI_CON

3D3V_S0
84.T3904.H11
Q5703 LMBT3904LT1G-GP
R5710 150KR2F-L-GP
R5711 200KR2F-L-GP
R5712 0R0402-PAD
8 CPU_DP1_HPD → HDMI_HPD_E
HDMI_HPD_B
R5709 10KR2J-3-GP

EMI Request:

ED5701 RCLAMP0524P-2-GP 75.00524.A73
HDMI_DATA1#_R_C
HDMI_DATA1_R_C
HDMI_DATA2#_R_C
HDMI_DATA2_R_C

ED5702 RCLAMP0524P-2-GP 75.00524.A73
HDMI_DATA0#_R_C
HDMI_DATA0_R_C
HDMI_CLK#_R_C
HDMI_CLK_R_C

ED5703 RCLAMP0524P-2-GP 75.00524.A73
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: A3
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Monday, June 27, 2016
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 58 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

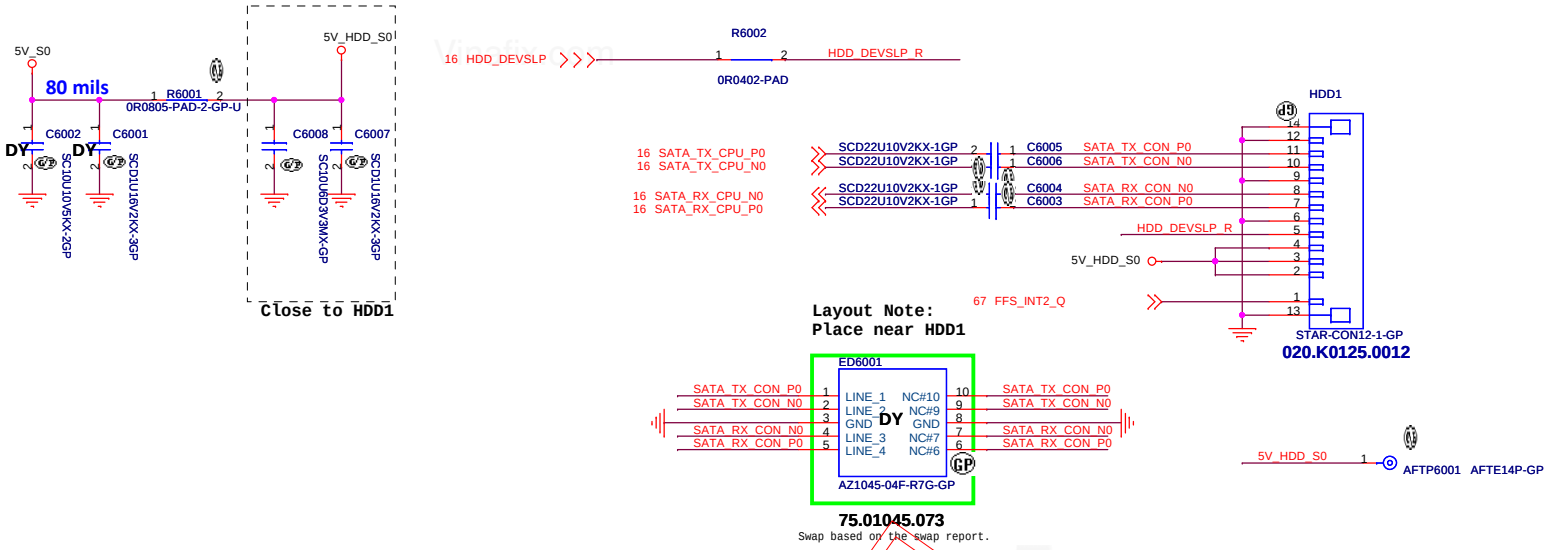
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 59 of 105

Main Func = HDD

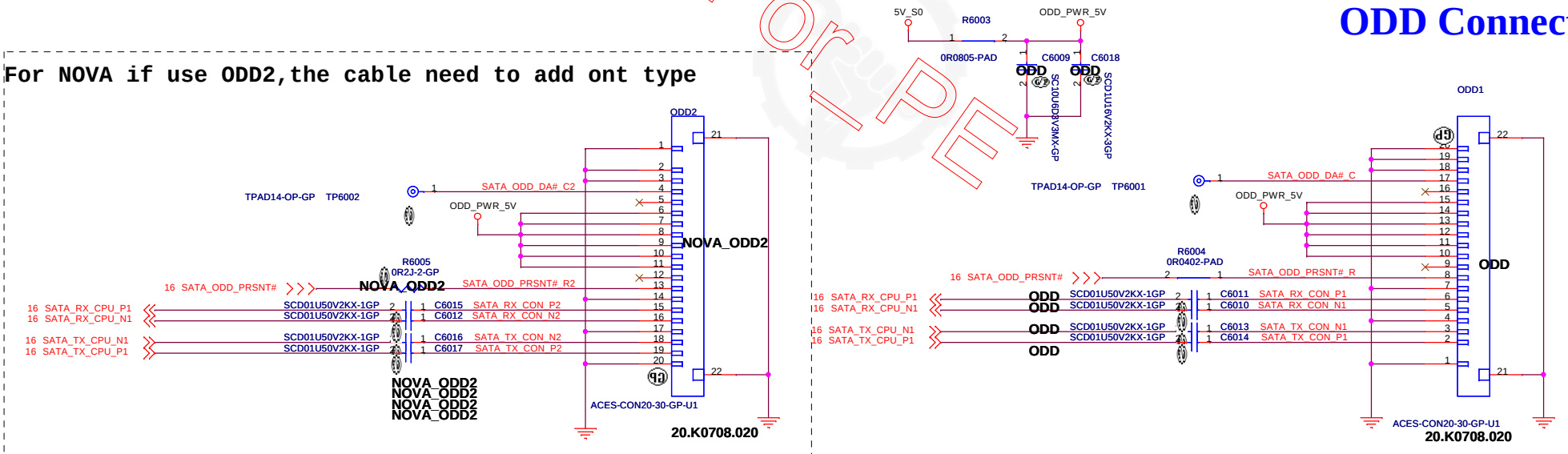
SATA HDD Connector



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector



<Core Design>

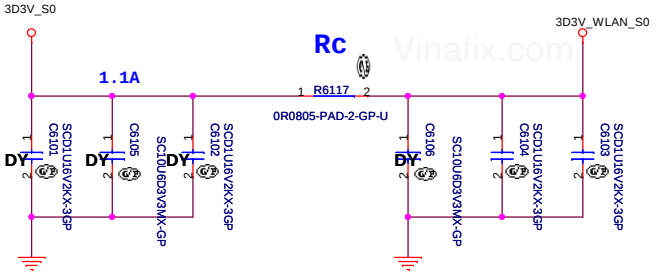
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

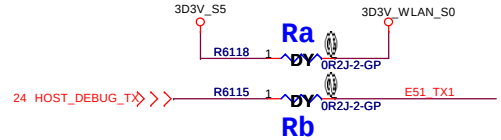
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 60 of 105

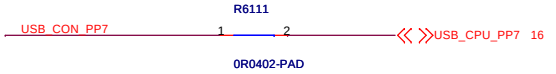
Main Func = WLAN

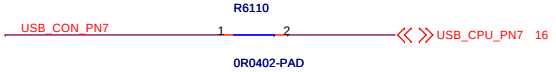


Reserved for NGFF Debug Card

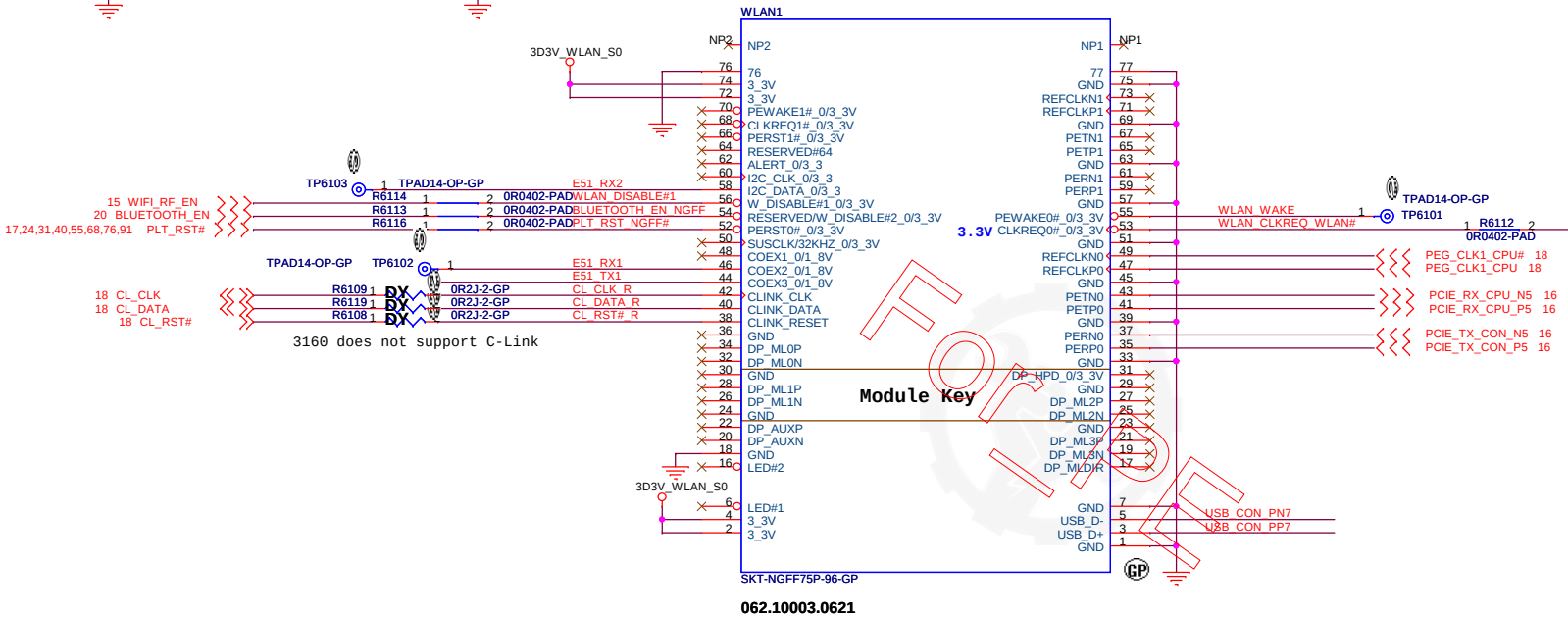


EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.



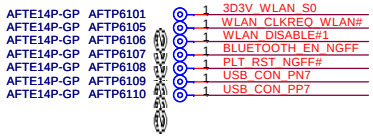


Note:pin 76 and pin 77 need contact to GND



062.10003.0621

Support: Intel Dual Band Wireless-AC 3160



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 61 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 62 of 105

(Blanking)

<Core Design>

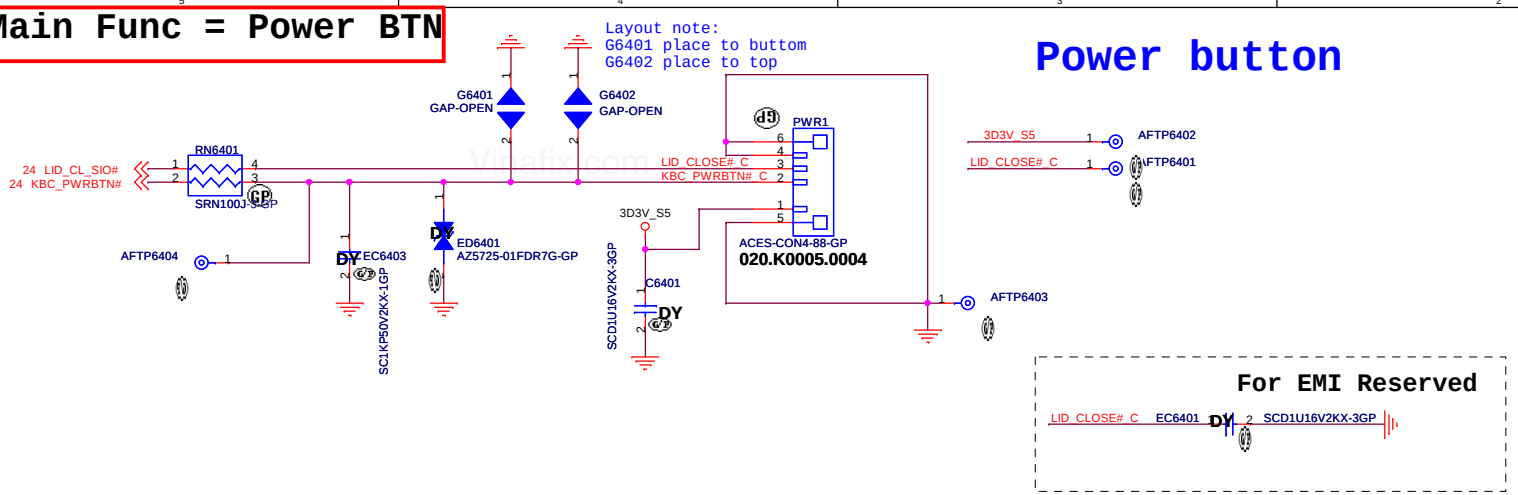
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

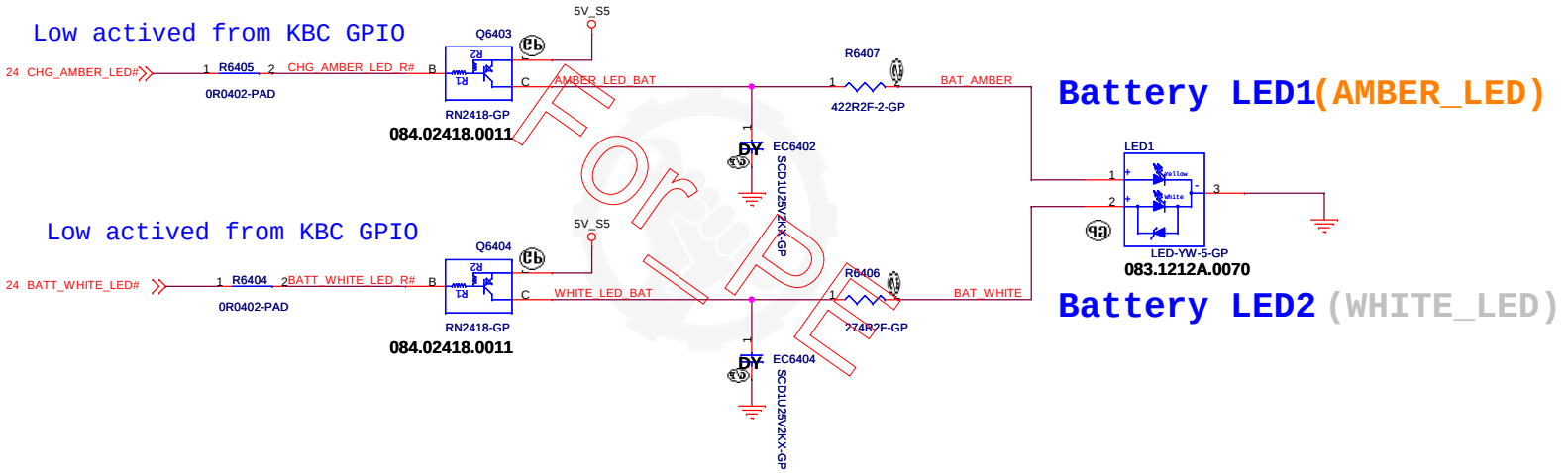
Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 63 of 105

Main Func = Power BTN

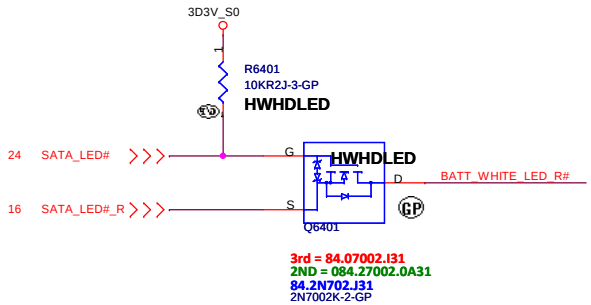


Main Func = Battery LED



Main Func = HDD LED

SATA HDD LED
LOW actived from PCH GPIO



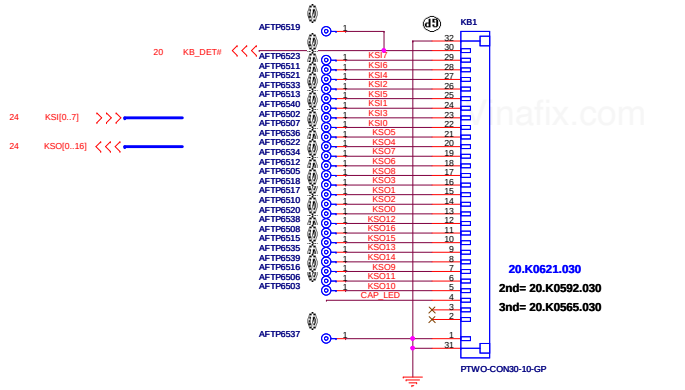
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Board&Power Button	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 64 of 105	

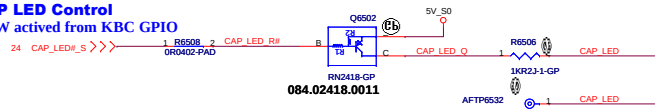
Main Func = KB

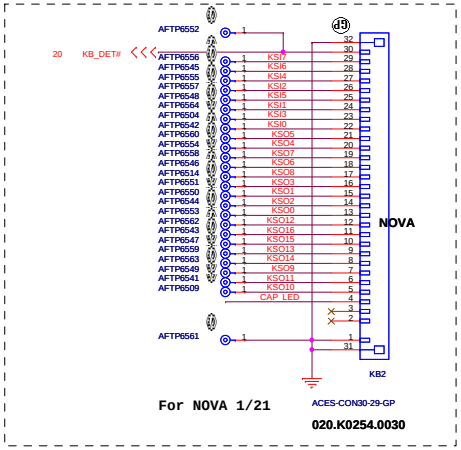
Internal Keyboard Connector



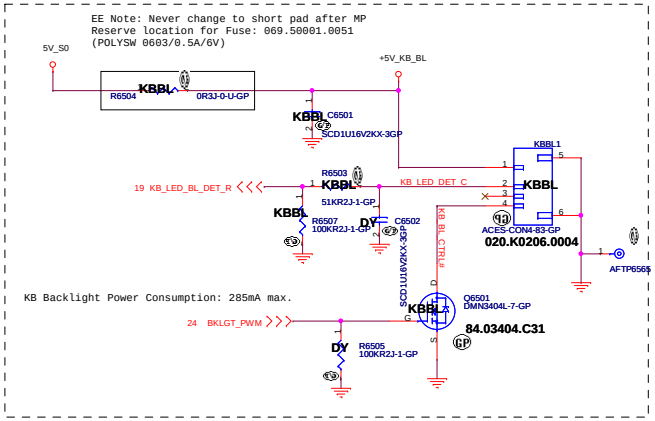
CAP LED Control

LOW actived from KBC GPIO

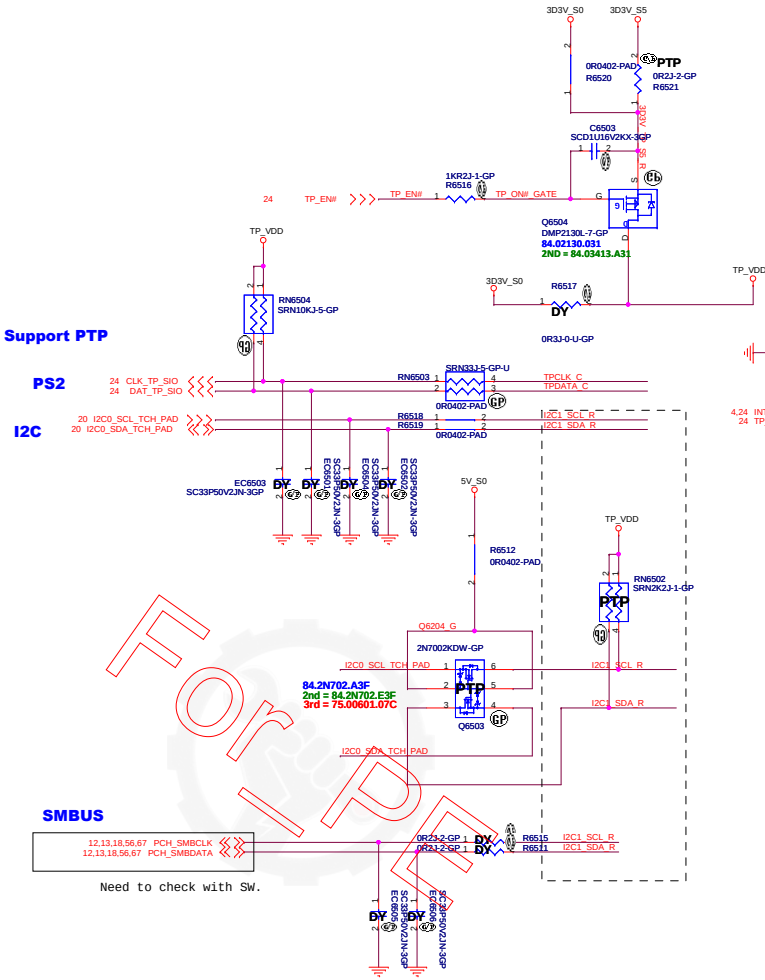


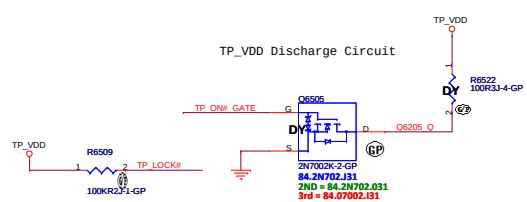


Keyboard Backlight (Reserved)

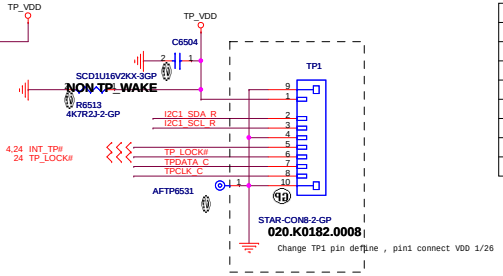


Main Func = TPAD



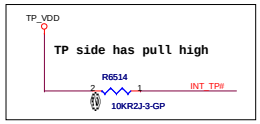


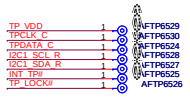
Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 65 of 105

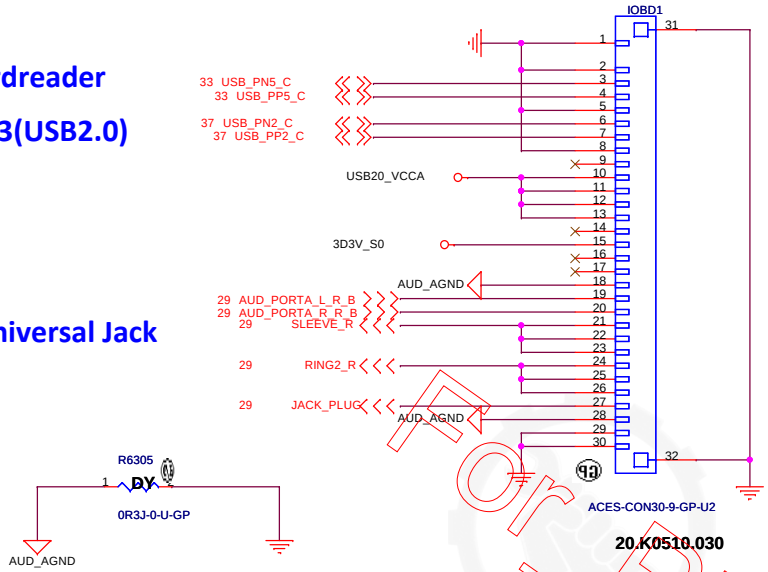
Main Func = IO Connector

I/O Board Connector

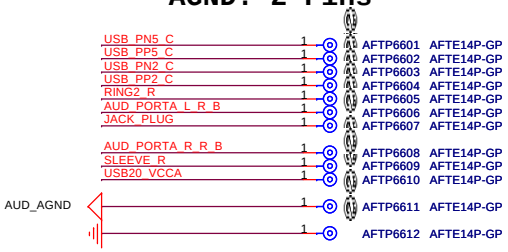
Cardreader

USB3(USB2.0)

Universal Jack



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

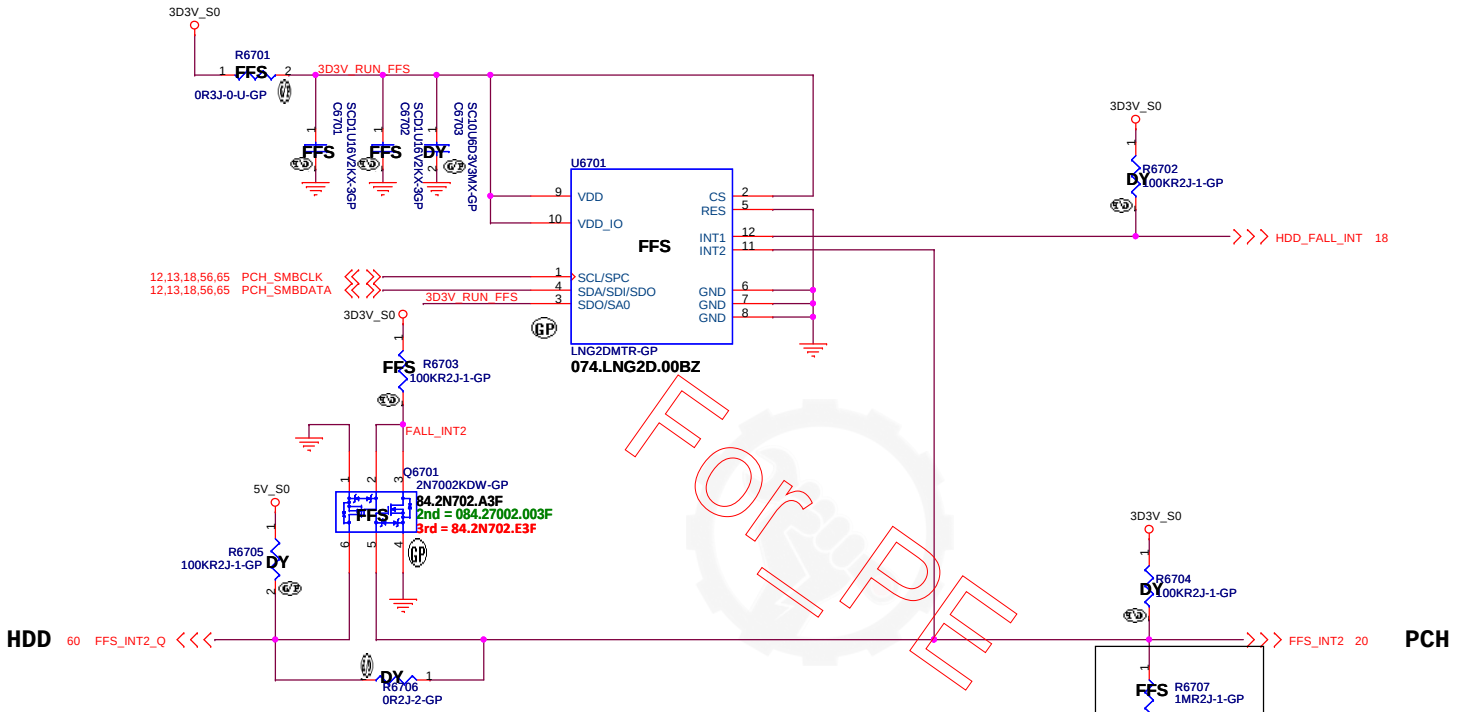
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 66 of 105

SSID = User.interface

Free Fall Sensor

DVT1 add FFS 2/18



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

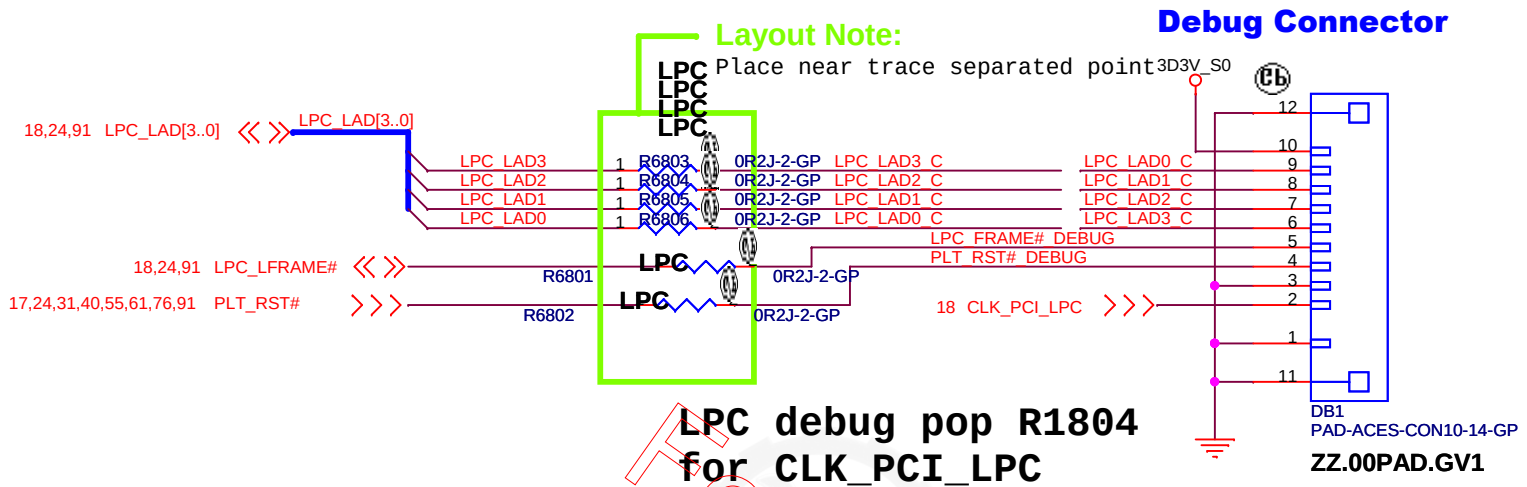
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 67 of 105

Main Func = Debug



LPC debug pop R1804 for CLK_PCI_LPC

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Monday, June 27, 2016 Sheet 68 of 105

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 69 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 70 of 105

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

RESERVED

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Thursday, June 16, 2016 Sheet 71 of 105

(Blanking)

<Core Design>

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Title

USB3.0 PORT

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Thursday, June 16, 2016 Sheet 72 of 105

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Thursday, June 16, 2016 Sheet 73 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 74 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 75 of 105

Main Func = dGPU

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A 1 OF 7

Table 3–5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

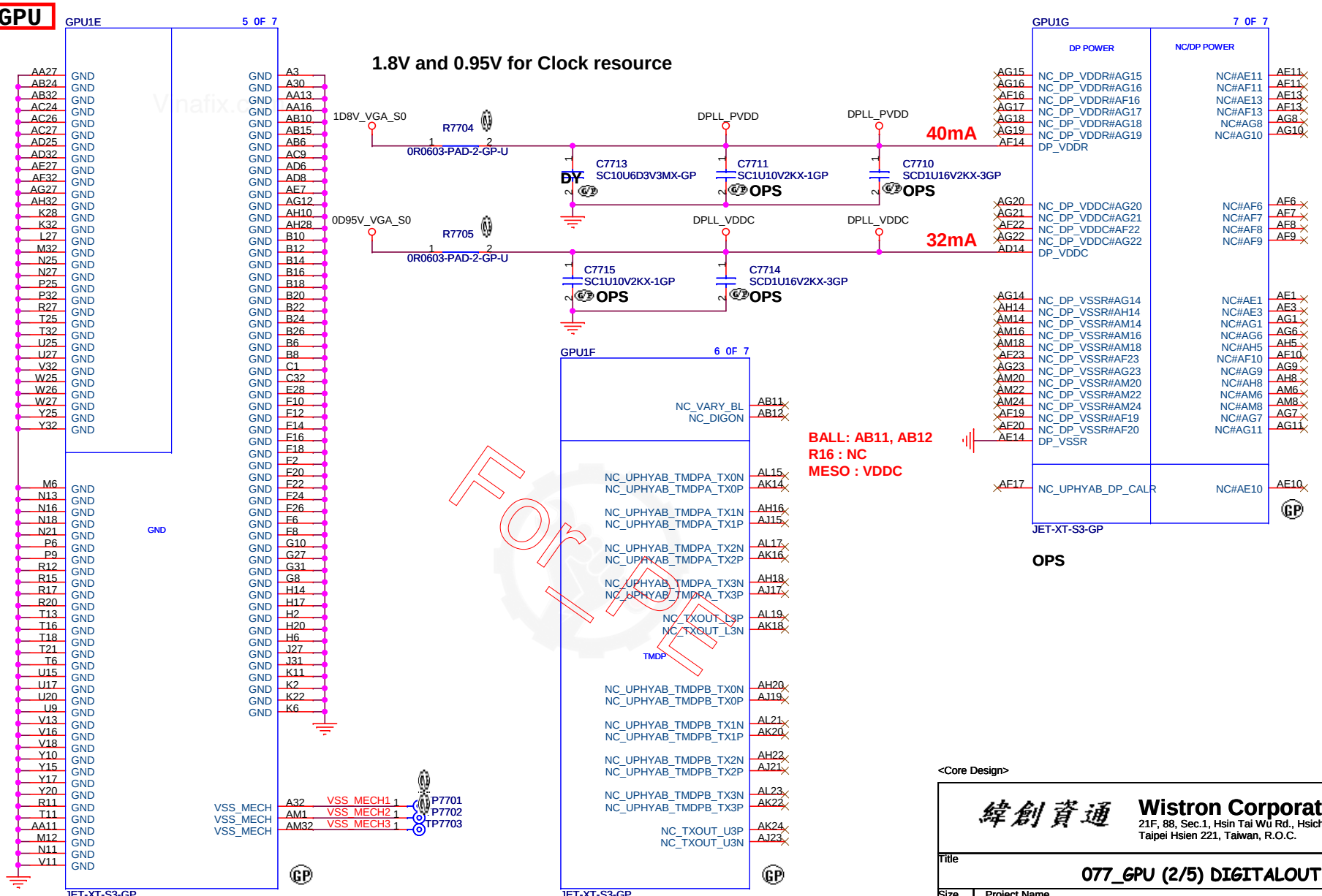
DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 076_GPU(1/5) PEG
Size | Project Name: <Project Name> | Rev
Date: Monday, June 27, 2016 Sheet 76 of 105

Main Func = dGPU

1.8V and 0.95V for Clock resource



<Core Design>

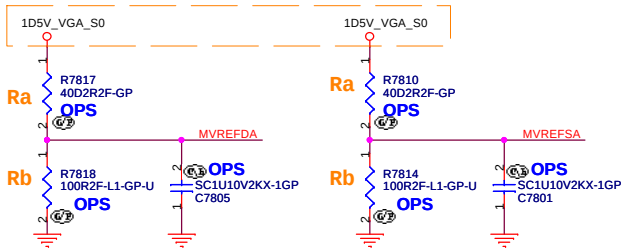
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	077_GPU (2/5) DIGITALOUT
Size	Project Name: Vegas SKL/KBL-U
Rev	X00
Date: Friday, June 24, 2016	Sheet 77 of 105

Main Func = dGPU

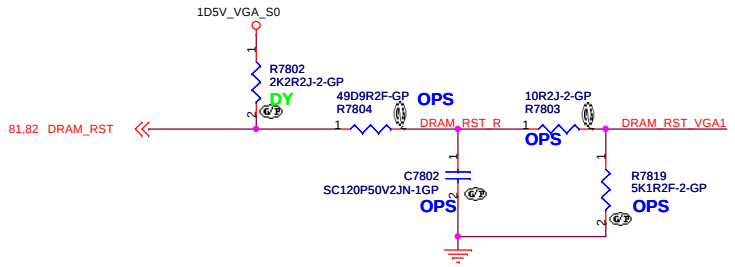
Please MVREF drivers and Caps close to ASIC

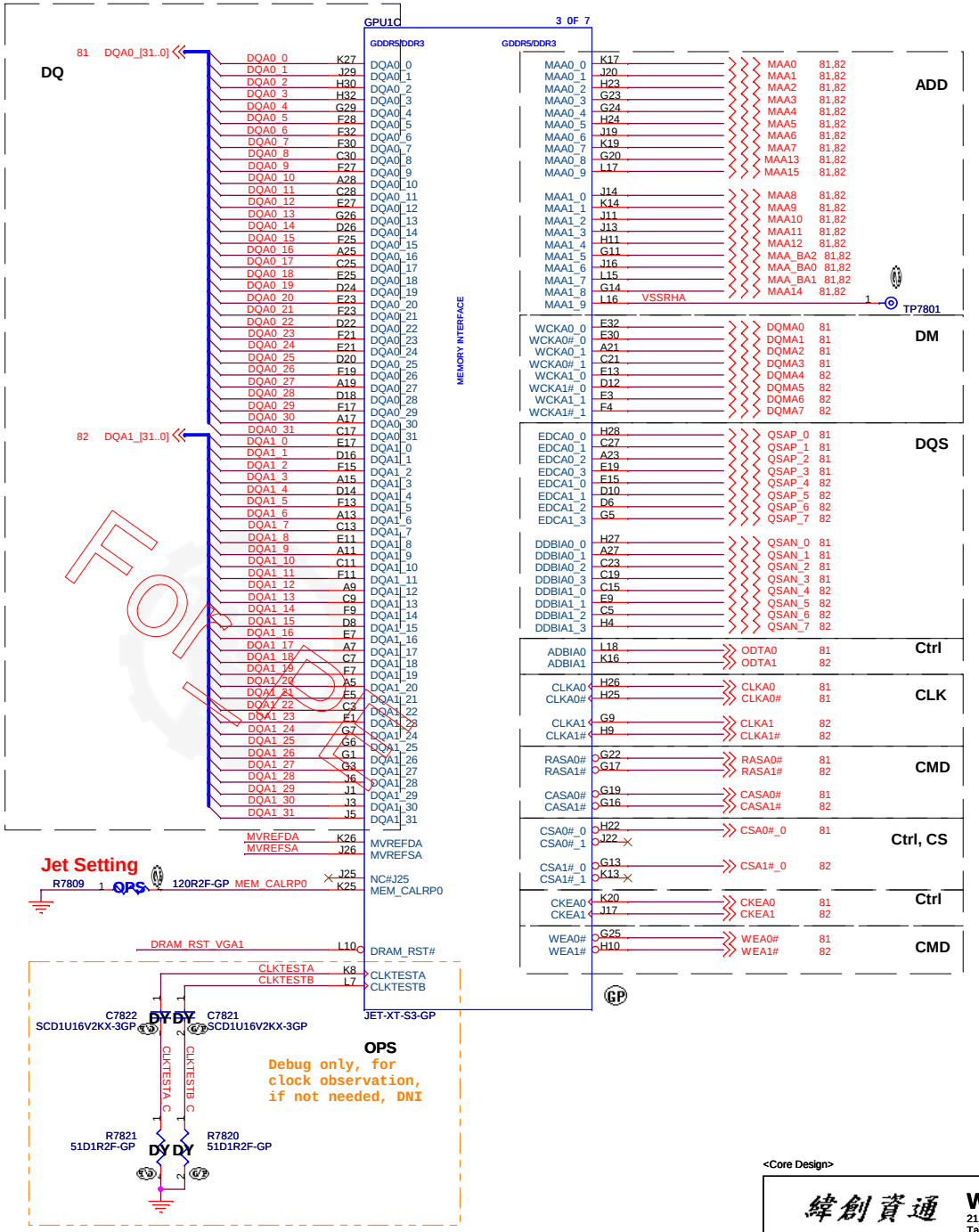
DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





<Core Design>

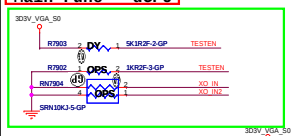
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

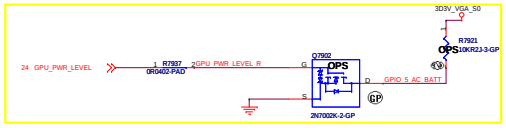
Title: 078_GPU (3/5) VRAM I/F

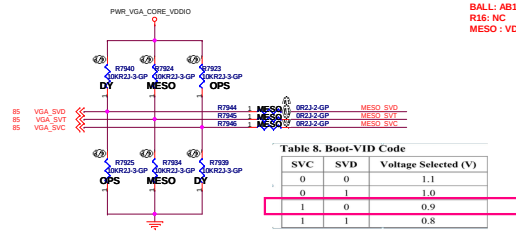
Size | Project Name: Vegas SKL/KBL-U | Rev

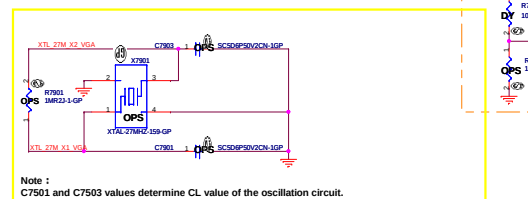
Date: Monday, June 27, 2016 Sheet 78 of 105

Main Func = dGPU



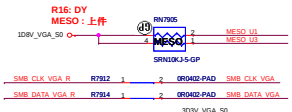


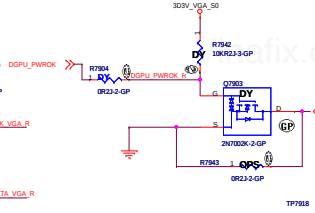




Note :
C7501 and C7503 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.

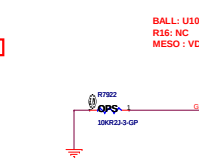
R16: DY
MESO : 上件





Pre-PWROK METAL VID CODES

SVC	SVD	Output Voltage
0	0	1.1
0	1	1.0
AMD suggestion	1	0	0.9
1	1	0.8



BALL: U10,T10,Y9,W10
R16: NC
MESO : VDDC

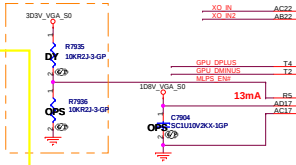
BALL: AB13, W9, AC14
R16: NC
MESO : VDDC

Table 8. Boot-VID Code

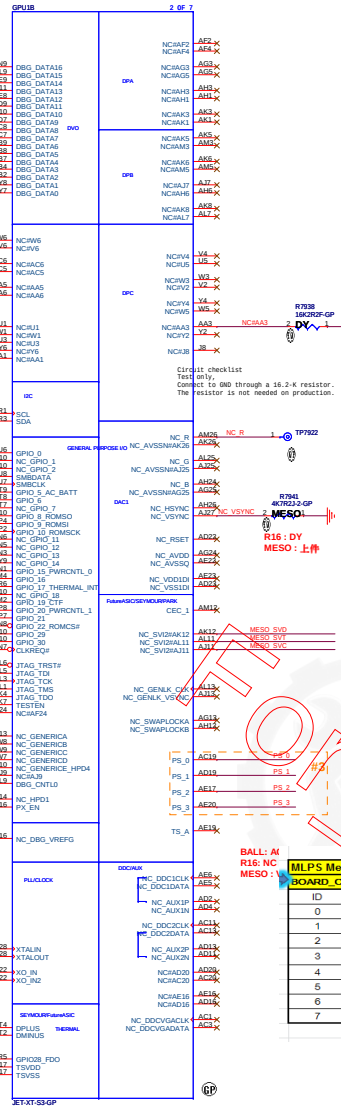
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

	SVID	PWR Sequencing
R16	R7919 R7920	PR8611 PC8607 / PR8612 PC8612

0: Enable MLPS, disable GPIO PINSTRAP
1: Disable MLPS, enable GPIO PINSTRAP



PINs for debug



#3

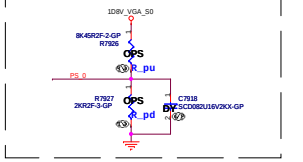
PS_0	R_pu	R_pd	Bits[3:1]	Size of the Prima
	NC	4750	000	128 MB
	8450	2000	001	256 MB
	4530	2000	010	64 MB
	6980	4990	011	Reserved
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

PS_1	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	PCIe GEN3 is not supported ; The CLKREQB power management capability is disabled
	8450	2000	001	PCIe GEN3 is supported ; The CLKREQB power management capability is disabled
	4530	2000	010	PCIe GEN3 is not supported ; The CLKREQB power management capability is enabled
	6980	4990	011	PCIe GEN3 is supported ; The CLKREQB power management capability is enabled
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

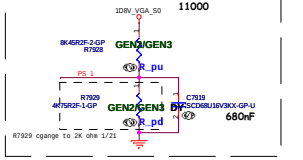
PS_2	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	Disable the external BIOS ROM device.
	8450	2000	001	N/A
	4530	2000	010	N/A
	6980	4990	011	N/A
	4530	4990	100	Enable the external BIOS ROM device.
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

AMD suggest Aperture Size = 256MB

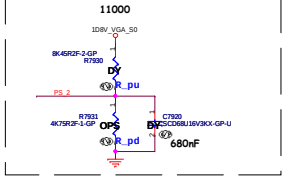
11001



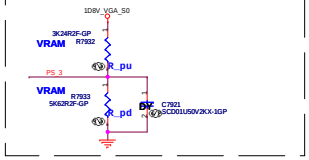
11000



11000



PS_3[3-1] => MEM_ID setting, need decide for AMD



MLPS Memory ID setting:

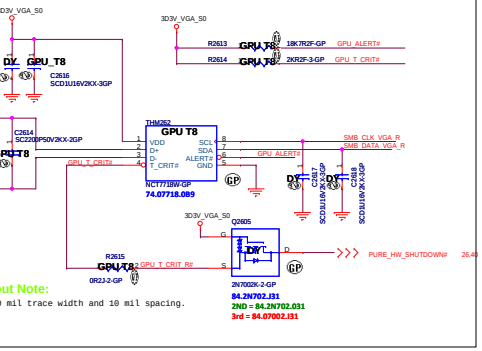
BOARD_CONFIG[2:0]		Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor P/N	SMT quantity	R_pu	R_pd
ID	[2:0]								
0	000	Samsung - DDR3L	256M x 16		2GB	K4W4G1646E-BC1A	4 pcs	NC	4750
1	001	Micron - DDR3L	256M x 16		2GB	MT41J256M16LY-091G:N	4 pcs	8450	2000
2	010	SK hynix - DDR3L	256M x 16		2GB	H5TC4G63EFR-N0C	4 pcs	4530	2000
3	011								
4	100								
5	101								
6	110								
7	111								

Resistor
4.75Kohm: PN/64.47515.6DL
8.45Kohm: PN/64.84515.6DL
2Kohm: PN/64.20015.6DL
4.53Kohm: PN/64.45315.6DL
6.98Kohm: PN/64.69815.6DL
4.99Kohm: PN/64.49915.6DL
3.24Kohm: PN/64.32415.6DL
3.4Kohm: PN/64.34015.6DL
5.62Kohm: PN/64.56215.6DL
10Kohm: PN/64.10025.6DL

Capacitor
680nF: PN/78.68421.5BL
82nF: PN/78.82321.2FL
10nF: PN/78.10324.L0L

OPS

GPU thermal sensor



Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 079_GPU (4/5) GPIO/STRAP
Size: | Project Name: Vegas SKL/KBL-U | Rev:
Date: Monday, June 27, 2016 | Sheet 79 of 105

Main Func = dGPU

AMD schematic Review need
10uF x 1, 2.2uFx5, 0.1uF x1, 0.01uF x1

1D5V_VGA_S0
C8001 SC10U6D3V3MX-GP OPS
C8003 SC1U10V2KX-1GP OPS
C8009 SC1U10V2KX-1GP DY
C8004 SC1U10V2KX-1GP OPS
1A

1D5V_VGA_S0
C8042 SC1U10V2KX-1GP DY
C8005 SC1U10V2KX-1GP DY
C8006 SC1U10V2KX-1GP DY
C8014 SCD01U50V2KX-1GP DY
SCD1U16V2KX-3GP C8007 DY

C8034 SC1U10V2KX-1GP OPS
C8031 SC1U10V2KX-1GP DY
C8032 SC1U10V2KX-1GP DY
C8033 SC1U10V2KX-1GP DY

1D8V_VGA_S0
C8017 SC1U10V2KX-1GP OPS
13mA

3D3V_VGA_S0
C8024 SC1U10V2KX-1GP OPS
25mA

GPU1D 4 OF 7

MEM I/O
H13 VDDR1
H16 VDDR1
H19 VDDR1
J10 VDDR1
J23 VDDR1
J24 VDDR1
J9 VDDR1
K10 VDDR1
K23 VDDR1
K24 VDDR1
K9 VDDR1
L11 VDDR1
L12 VDDR1
L13 VDDR1
L20 VDDR1
L21 VDDR1
L22 VDDR1

LEVEL TRANSLATION
AA20 VDD_CT
AA21 VDD_CT
AB20 VDD_CT
AB21 VDD_CT

I/O
AA17 VDDR3
AA18 VDDR3
AB17 VDDR3
AB18 VDDR3
V12 NC_VDDR4#V12
Y12 NC_VDDR4#Y12
U12 NC_VDDR4#U12

PLL
MPV18 90mA L8 MPLL_PVDD
SPV18 75mA H7 SPLL_PVDD
SPV10 100mA H8 SPLL_VDDC
J7 SPLL_PVSS

PCIE
PCIE_PVDD AM30 0.1A
NC#AB23 AB23
NC#AC23 AC23
NC#AD24 AD24
NC#AE24 AE24
NC#AE25 AE25
NC#AE26 AE26
NC#AF25 AF25
NC#AG26 AG26
PCIE_VDDC L23 2.5A
PCIE_VDDC L24
PCIE_VDDC L25
PCIE_VDDC L26
PCIE_VDDC M22
PCIE_VDDC N22
PCIE_VDDC N23
PCIE_VDDC N24
PCIE_VDDC R22
PCIE_VDDC T22
PCIE_VDDC U22
PCIE_VDDC V22

CORE
VDDC AA15
VDDC N15
VDDC N17
VDDC R13
VDDC R16
VDDC R18
VDDC Y21
VDDC T12
VDDC T15
VDDC T17
VDDC T20
VDDC U13
VDDC U16
VDDC U18
VDDC V21
VDDC V15
VDDC V17
VDDC V20
VDDC Y13
VDDC Y16
VDDC Y18
VDDC AA12
VDDC M11
VDDC N12
VDDC U11

POWER
BIF_VDDC R21 1.4A
BIF_VDDC U21

ISOLATED CORE I/O
VDDCI M13 5A
VDDCI M15
VDDCI M16
VDDCI M17
VDDCI M18
VDDCI M20
VDDCI M21
VDDCI N20

JET-XT-S3-GP

1D8V_VGA_S0
C8008 SC1U10V2KX-1GP DY
C8002 SC10U6D3V3MX-GP OPS

0D95V_VGA_S0
C8010 SC10U6D3V3MX-GP DY
C8016 SC10U6D3V3MX-GP OPS

AMD schematic Review need 10uF x 2, 1uFx3, 0.1uF x2
0D95V_VGA_S0
C8011 SCD1U16V2KX-3GP OPS
C8012 SCD1U16V2KX-3GP OPS
C8013 SC1U10V2KX-1GP OPS
C8015 SC1U10V2KX-1GP OPS
C8057 SC1U10V2KX-1GP OPS

AMD ORB 10U x 6 2.2U x 16
LF145M 4.7U x 6 1U x 20
VGA_CORE
C8018 SC1U10V2KX-1GP OPS
C8019 SC1U10V2KX-1GP OPS
C8020 SC1U10V2KX-1GP OPS
C8021 SC1U10V2KX-1GP OPS
C8022 SC1U10V2KX-1GP OPS
C8023 SC1U10V2KX-1GP OPS

NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
VGA_CORE
C8025 SC1U10V2KX-1GP OPS
C8026 SC1U10V2KX-1GP OPS
C8027 SC1U10V2KX-1GP OPS
C8028 SC1U10V2KX-1GP OPS
C8029 SC1U10V2KX-1GP OPS
C8030 SC1U10V2KX-1GP OPS

VGA_CORE
C8035 SC1U10V2KX-1GP OPS
C8036 SC1U10V2KX-1GP OPS
C8037 SC1U10V2KX-1GP OPS
C8058 SC1U10V2KX-1GP OPS
C8059 SC1U10V2KX-1GP OPS
C8060 SC1U10V2KX-1GP OPS

Memory phase lock loop power: Dedicated analogue power in for memory PLLs
1D8V_VGA_S0
L8001 MMZ1005S241C-GP OPS
MPV18
C8043 SC10U6D3V3MX-GP OPS
C8044 SC10U6D3V3MX-GP OPS
C8045 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated analogue power pin for engine PLL
1D8V_VGA_S0
L8002 BLM15BD121SN1D-GP OPS
SPV18
C8053 SC10U6D3V3MX-GP OPS
C8054 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated digital power pin for engine PLL
0D95V_VGA_S0
L8003 BLM15BD121SN1D-GP OPS
SPV10
C8055 SC1U10V2KX-1GP OPS
SCD1U16V2KX-3GP C8056 OPS

0D95V_VGA_S0
C8065 SC1U10V2KX-1GP OPS
VGA_CORE
C8066 SC22U6D3V3MX-1-GP OPS
C8061 SC1U10V2KX-1GP OPS
C8062 SC1U10V2KX-1GP OPS

AMD ORB 10U x 2 1U x 3 0.1U x2
LF145M 4.7U x 2 1U x 3 0.1U x 2
VGA_CORE
C8046 SCD1U16V2KX-3GP OPS
C8047 SCD1U16V2KX-3GP OPS
C8048 SC1U10V2KX-1GP OPS
C8049 SC1U10V2KX-1GP OPS
C8050 SC1U10V2KX-1GP OPS

VGA_CORE
C8051 SC4D7U6D3V3KX-GP OPS
C8052 SC4D7U6D3V3KX-GP OPS

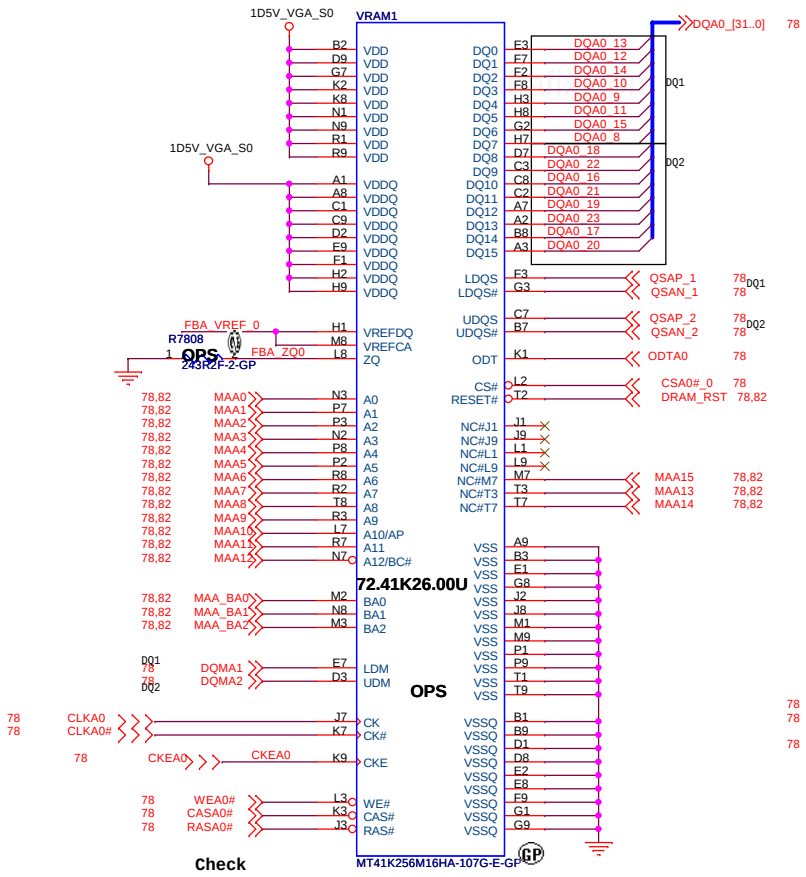
VGA_CORE
C8040 SC10U6D3V3MX-GP OPS
C8041 SC10U6D3V3MX-GP OPS
C8063 SC10U6D3V3MX-GP OPS
C8064 SC10U6D3V3MX-GP OPS
C8038 SC10U6D3V3MX-GP OPS
C8039 SC10U6D3V3MX-GP OPS

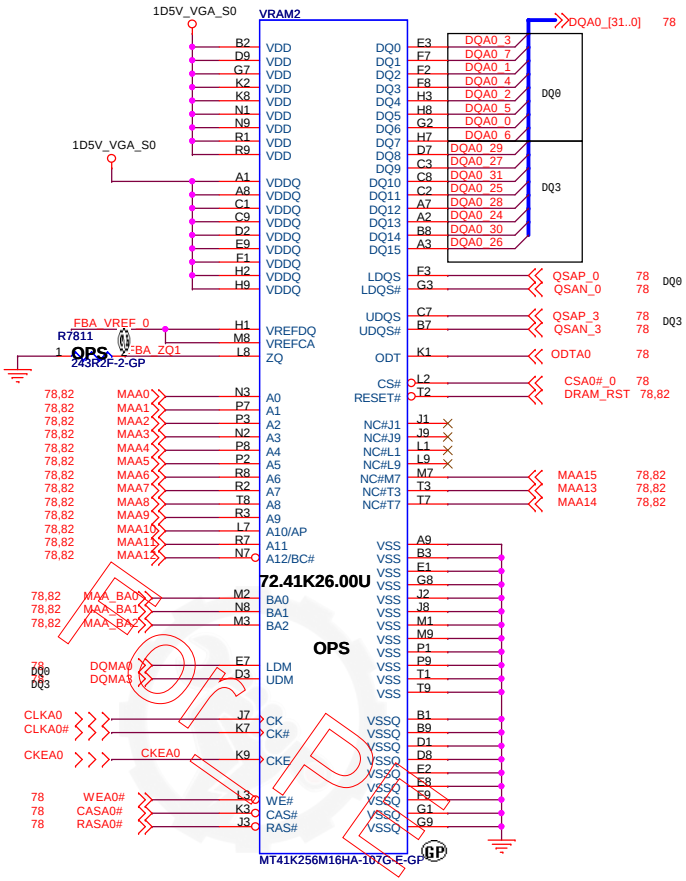
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

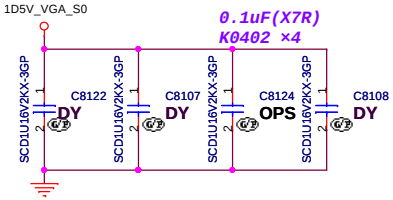
Title: 080_GPU (5/5) PWR/GND
Size | Project Name: <Project Name> | Rev
Date: Thursday, June 16, 2016 Sheet 80 of 105

Main Func = Vram (DDR3L)

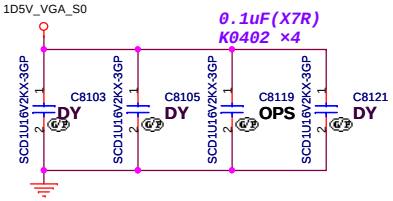




Place close VRAM1VDDQ ball

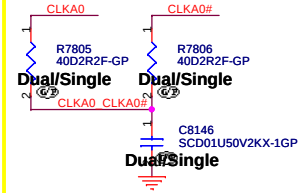


Place close VRAM2 VDD ball

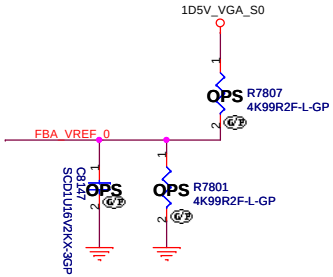


R7805 R7810

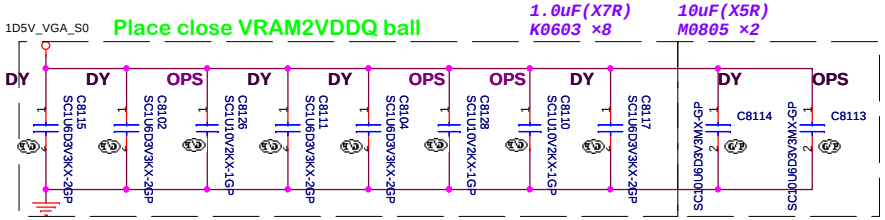
Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



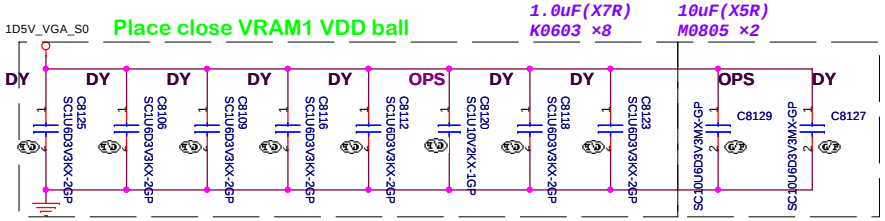
Frame Buffer Patition A-Lower Half



Place close VRAM2VDDQ ball



Place close VRAM1 VDD ball



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Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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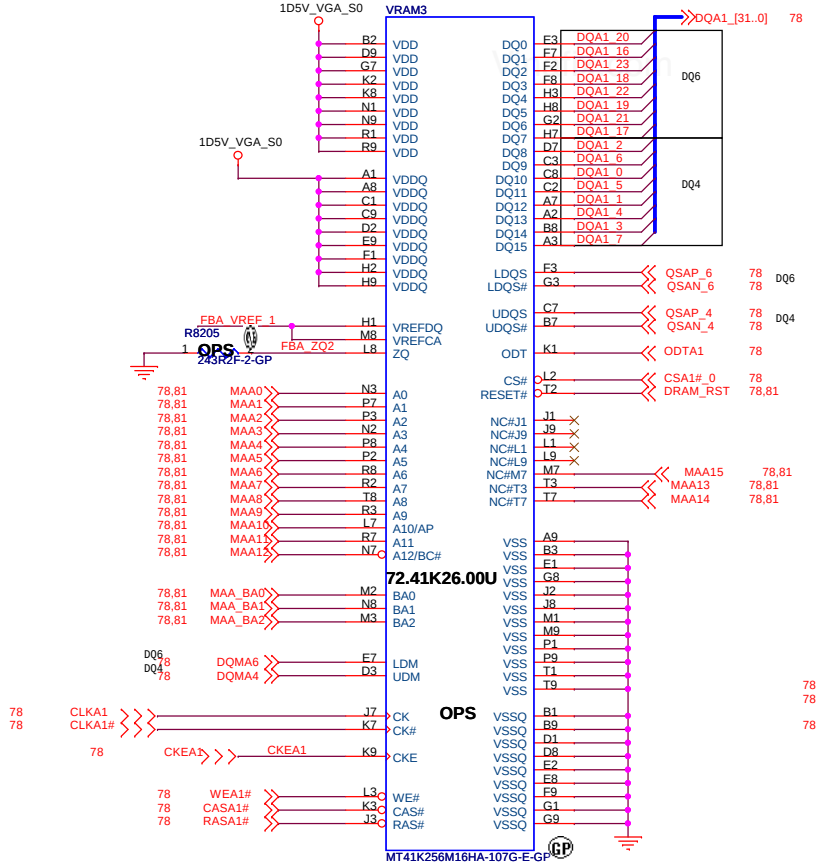
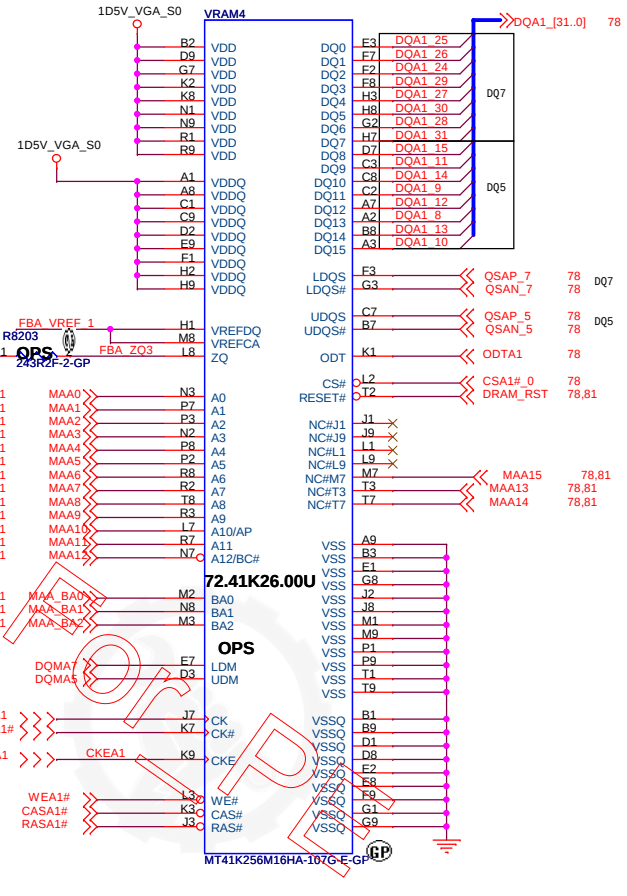
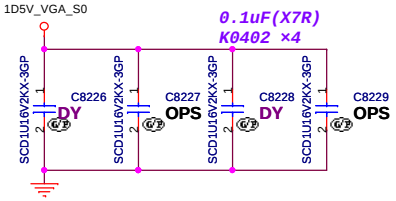
Main Func = Vram (DDR3L)

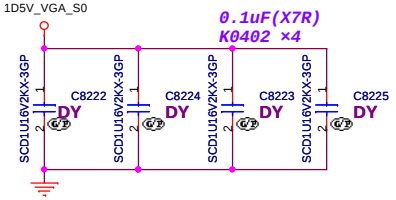




Place close VRAM3VDDQ ball

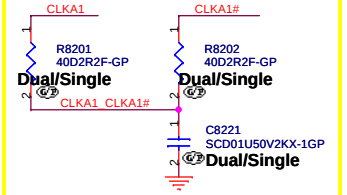


Place close VRAM4VDDQ ball

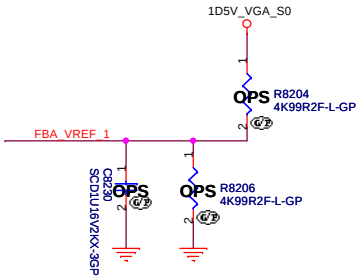


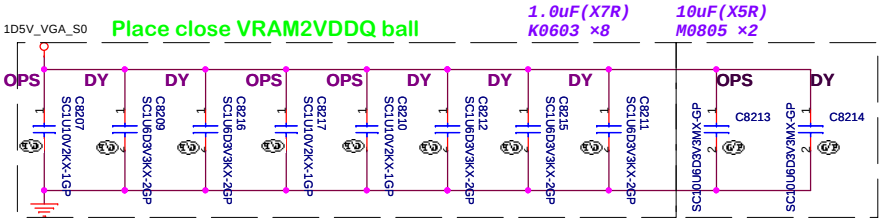
R7905 R7910

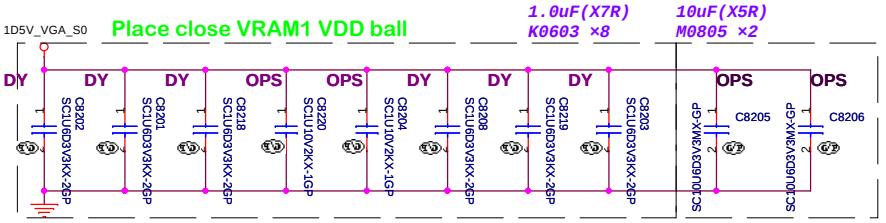
Single Rank, 40.2 Ohm
Dual Rank, 80.6 Ohm



Frame Buffer Patition A-Lower Half







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Title: GPU-VRAM3,4 (2/4)

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Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 83 of 105

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Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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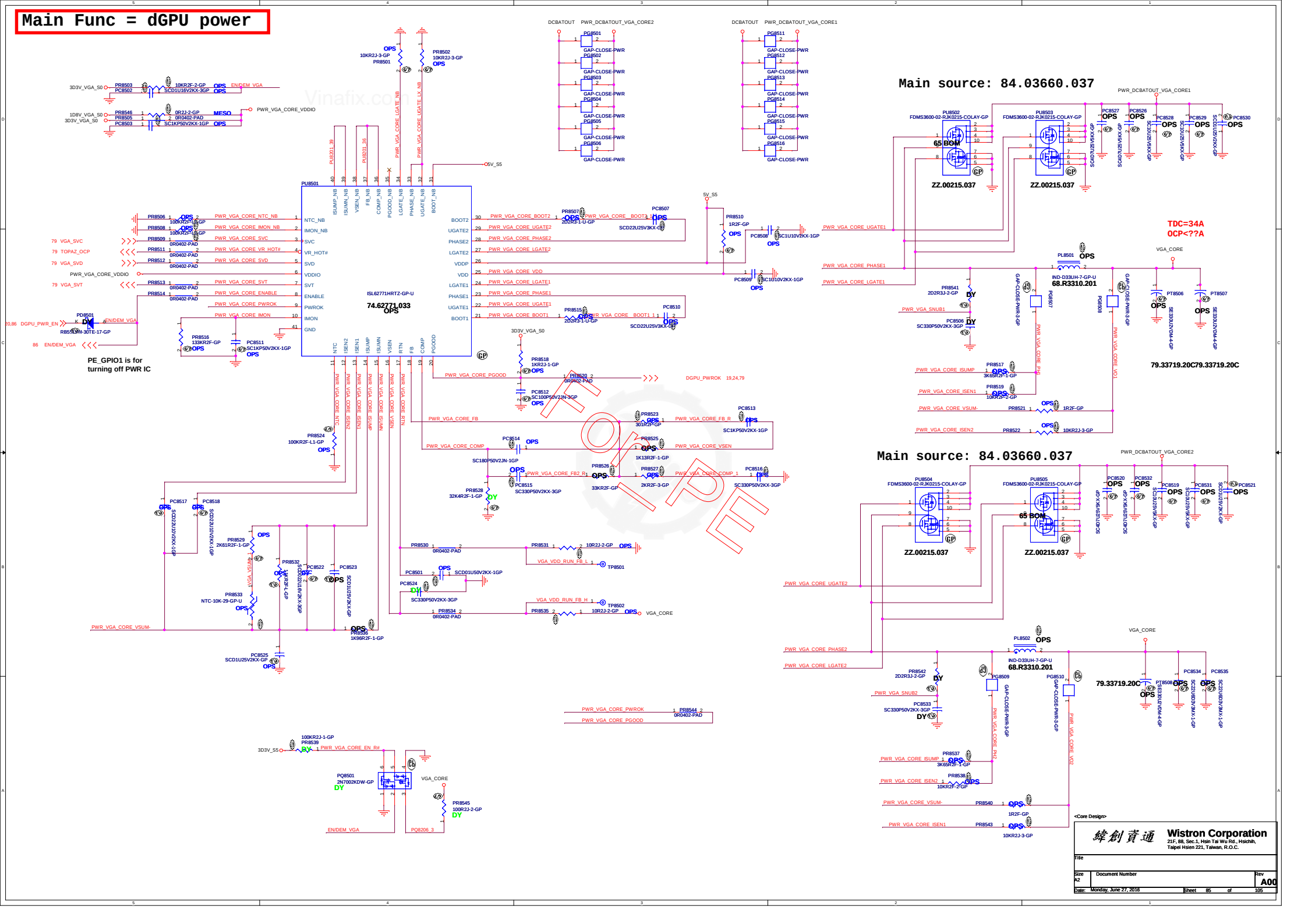
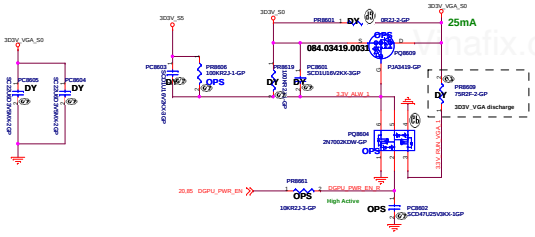
Main Func = dGPU power



Main Func = dGPU

3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D5V_VGA_S0

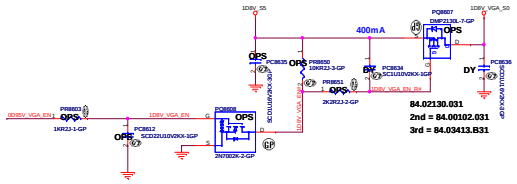
=> VGA_CORE

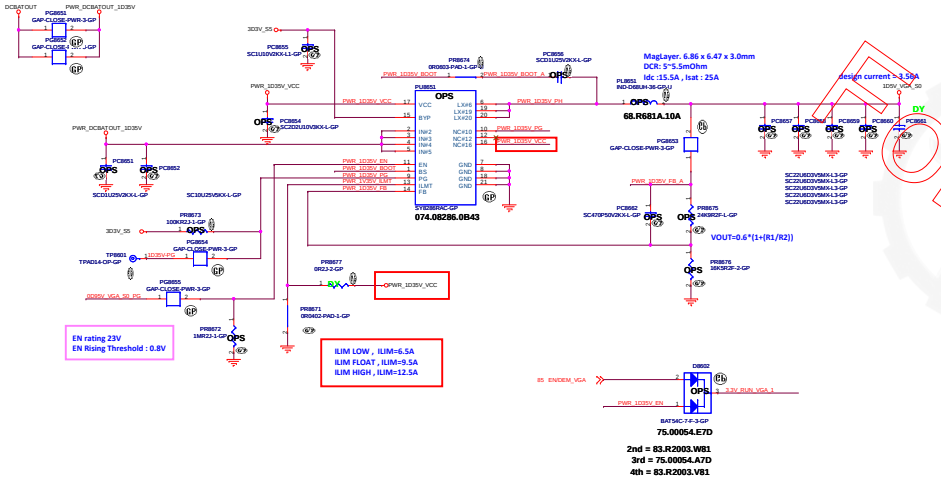
All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

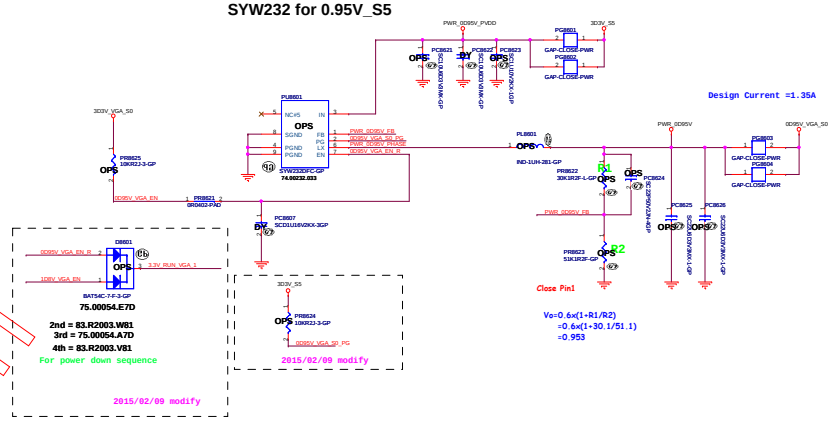
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

1D8V_VGA_S0





SYW232 for 0.95V_S5



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Title: GPU Discrete Power

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

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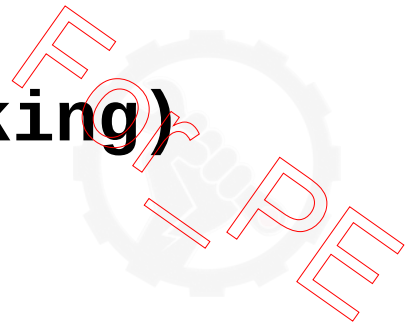

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Title

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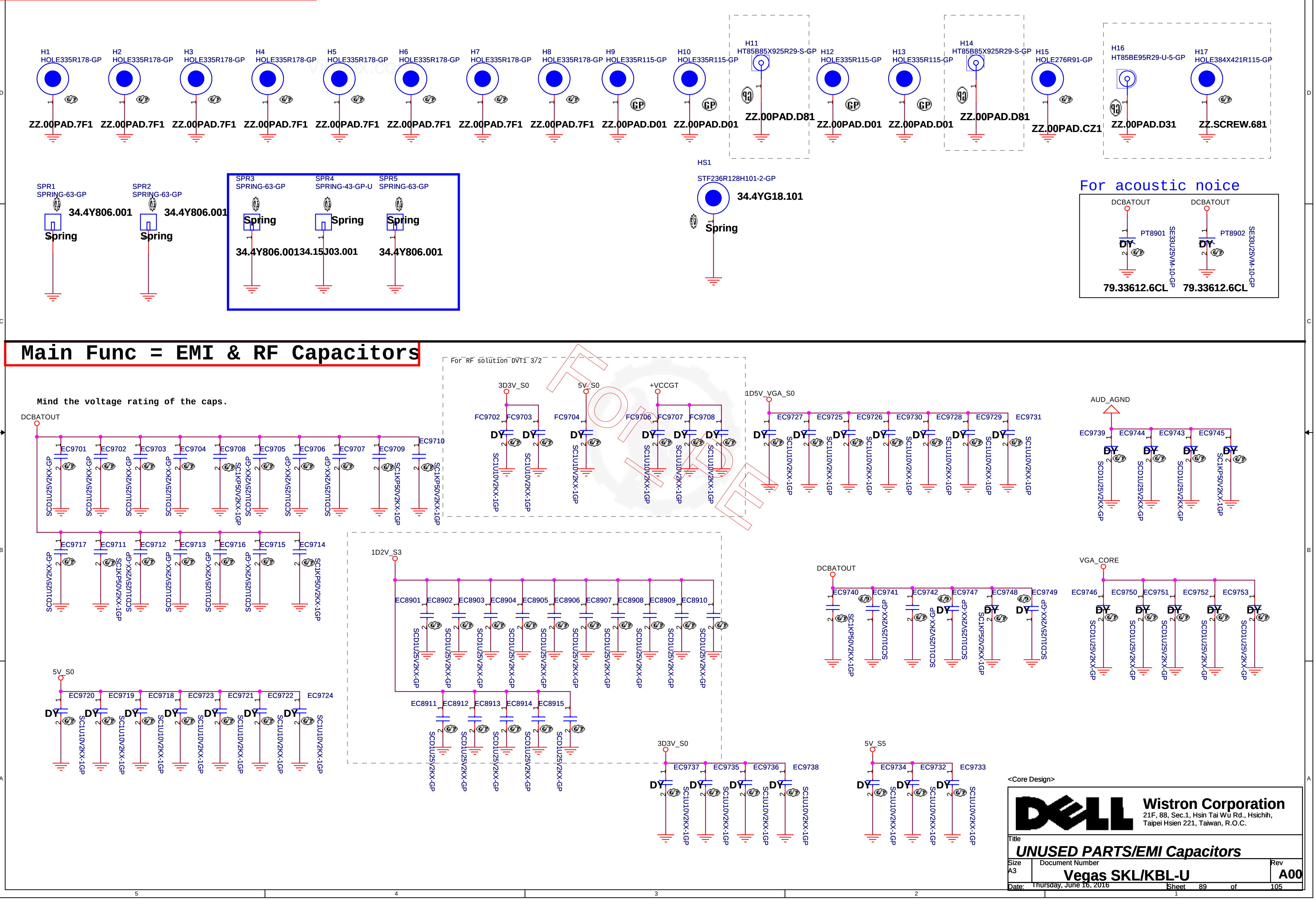
Main Func = UnusedParts

Main Func = EMI & RF Capacitors



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Title: *UNUSED PARTS/EMI Capacitors*

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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Title

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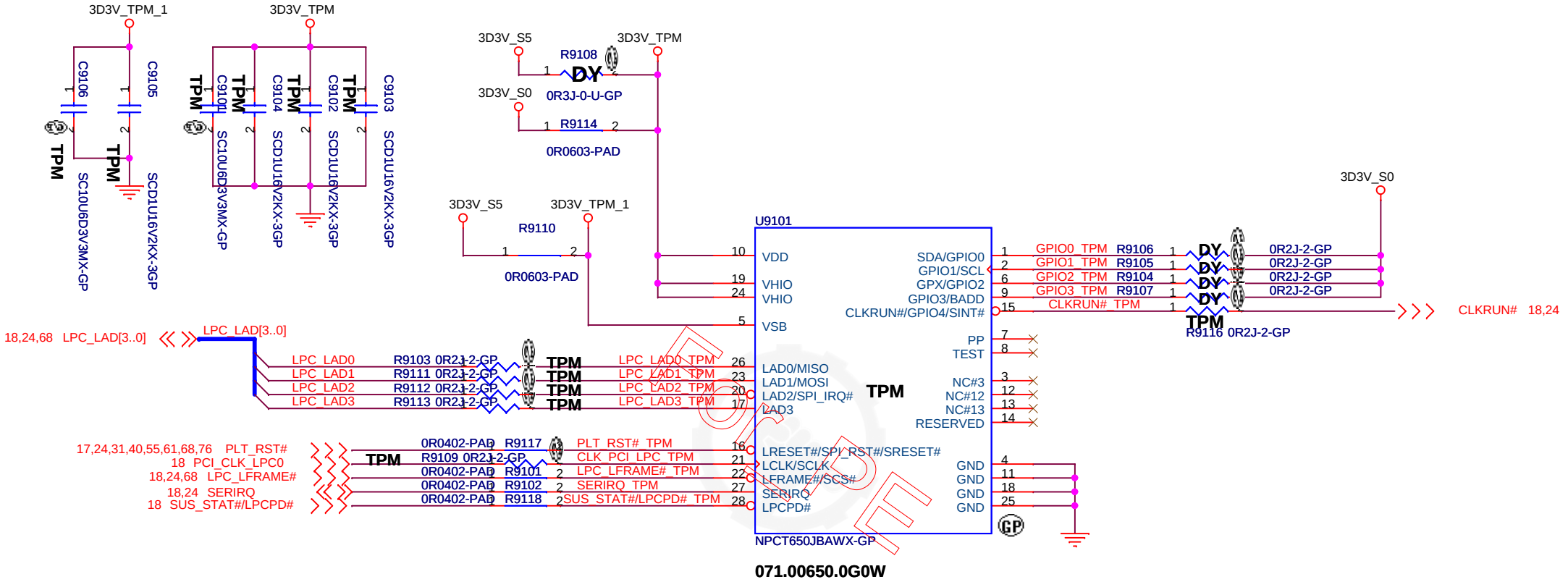
SSID = TPM



1.6.2 LPC Host Interface

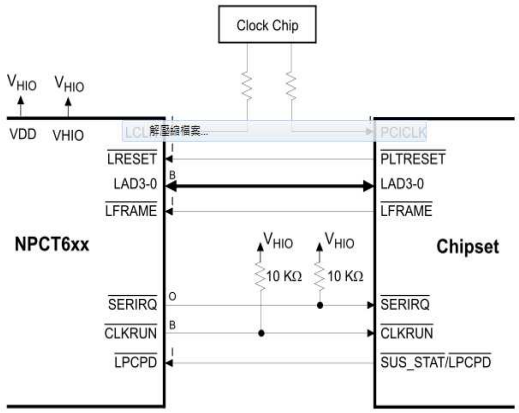


Figure 1-6. Host-LPC Interface Connection

<Core Design>

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Title: *TPM*		
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
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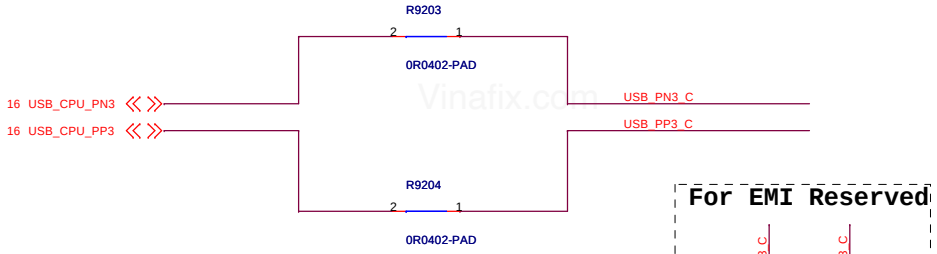
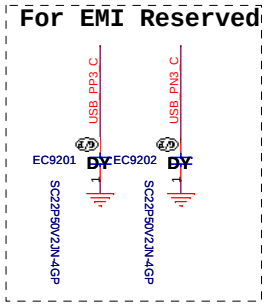
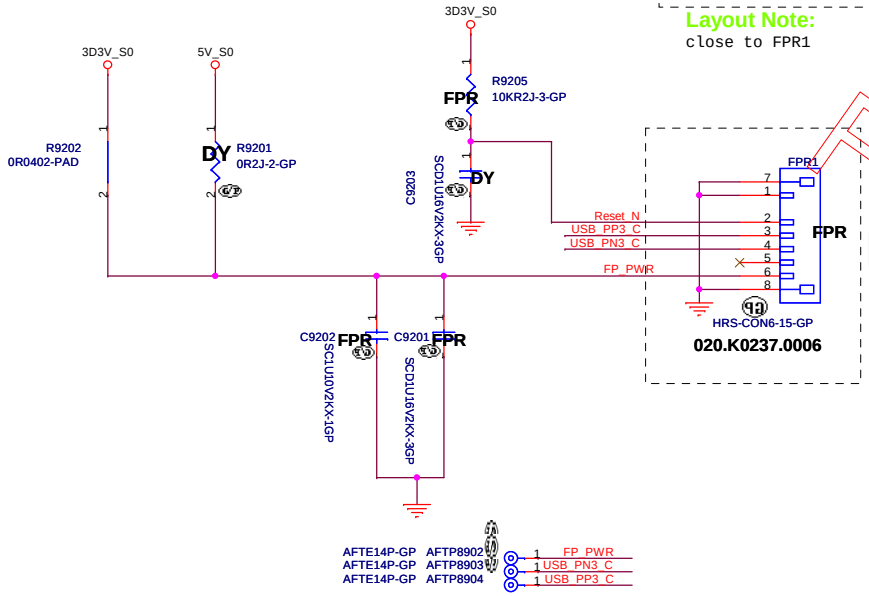
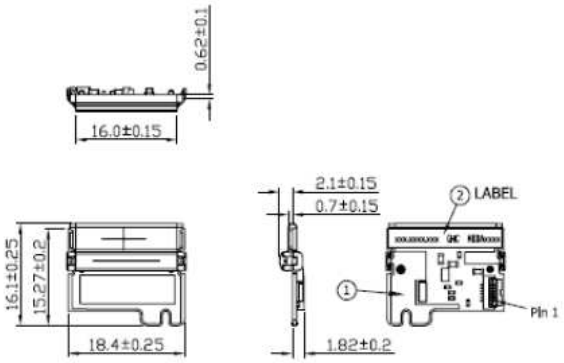
SSID = Finger Print





Layout Note:
close to FPR1

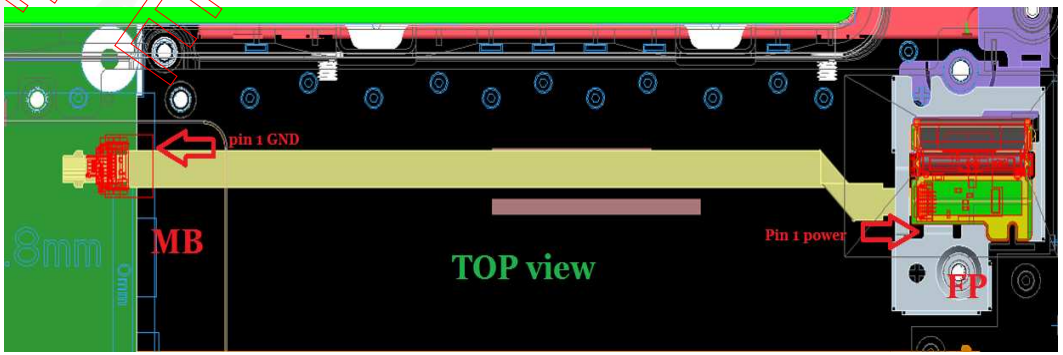




FingerPrint Pin Assignments.

Pin 1 = 3.3Vin
Pin 2 = GND
Pin 3 = D-
Pin 4 = D+
Pin 5 = Reset_N
Pin 6 = GND

Note :
Module:
1.Sensor Type:Semiconductor
2.Interface:USB 1.0 and 2.0 Full Speed



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Title: Finger Print

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Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

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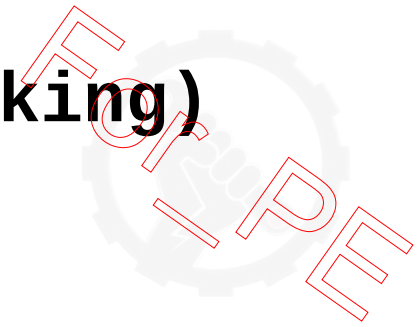

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

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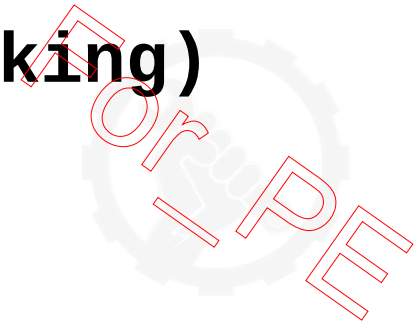

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Title: ***LVDS_Switch***

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A4	**Vegas SKL/KBL-U**	**A00**

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Title: CRT_Switch

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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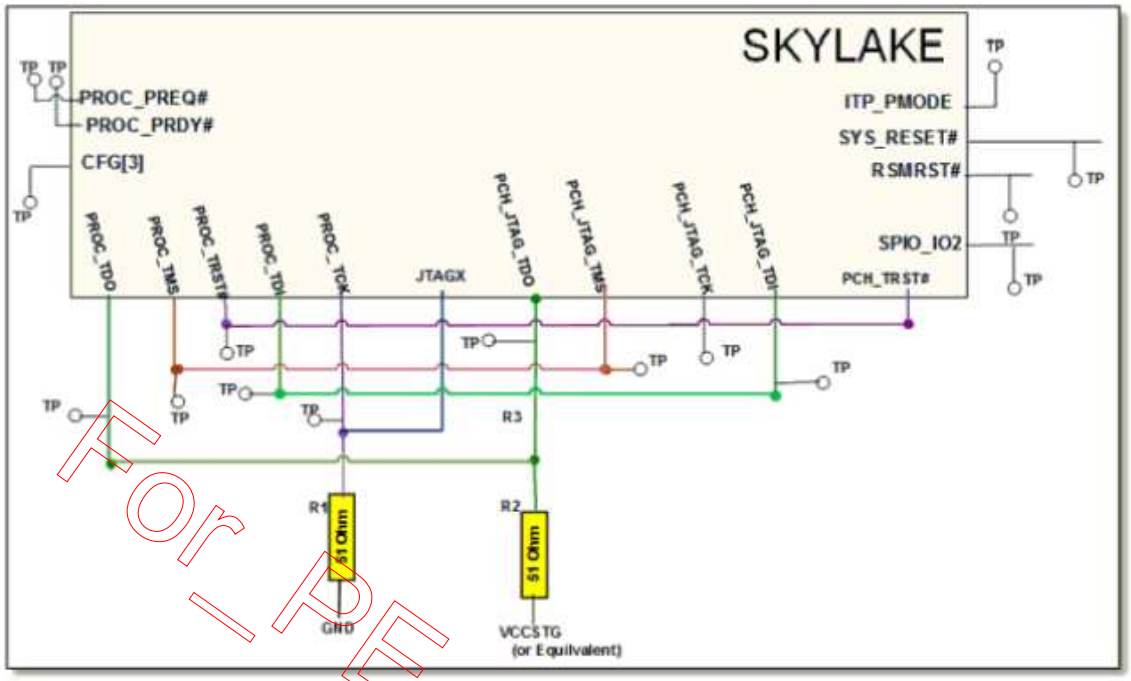
PCH_JTAG_TMS
XDP_TMS
test point

PCH_JTAG_TDI
XDP_TDI
test point

XDP_TCLK
XDP_TCK_JTAGX
test point

XDP_TDO_CPU
PCH_JTAG_TDO
test point



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Title
CPU_XDP;PCH_XDP

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A4	Vegas SKL/KBL-U	A00

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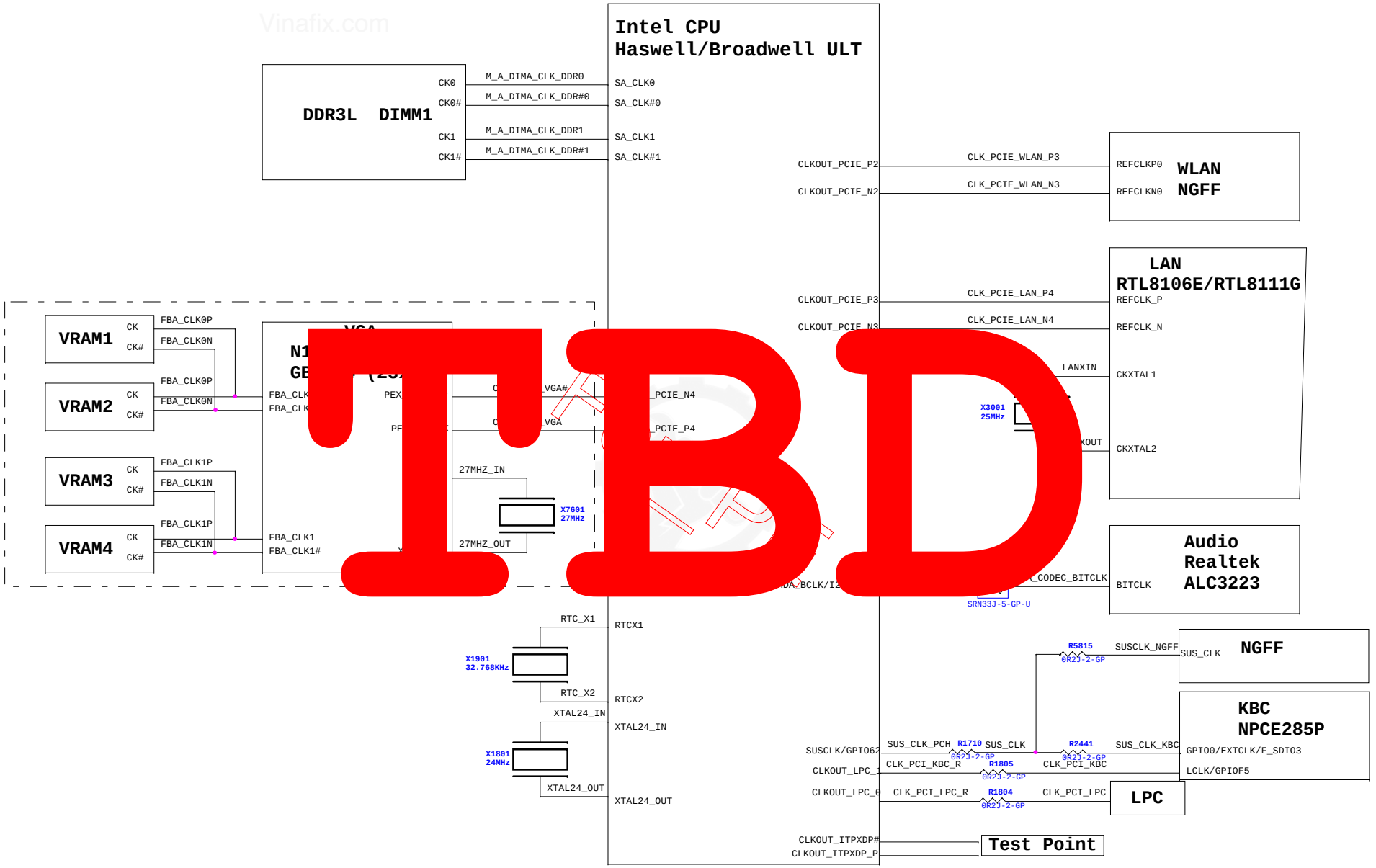
CLK Block Diagram



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Title	CLK Block Diagram	
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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: Change History

Size	Document Number	Rev
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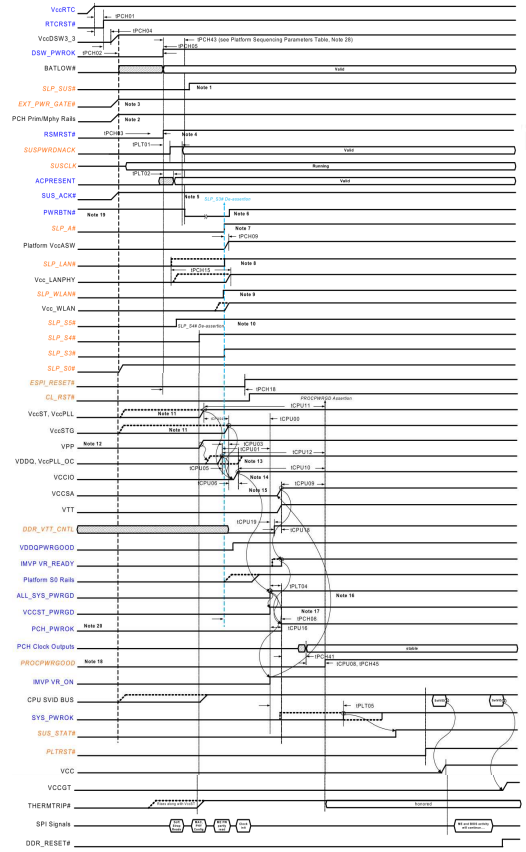
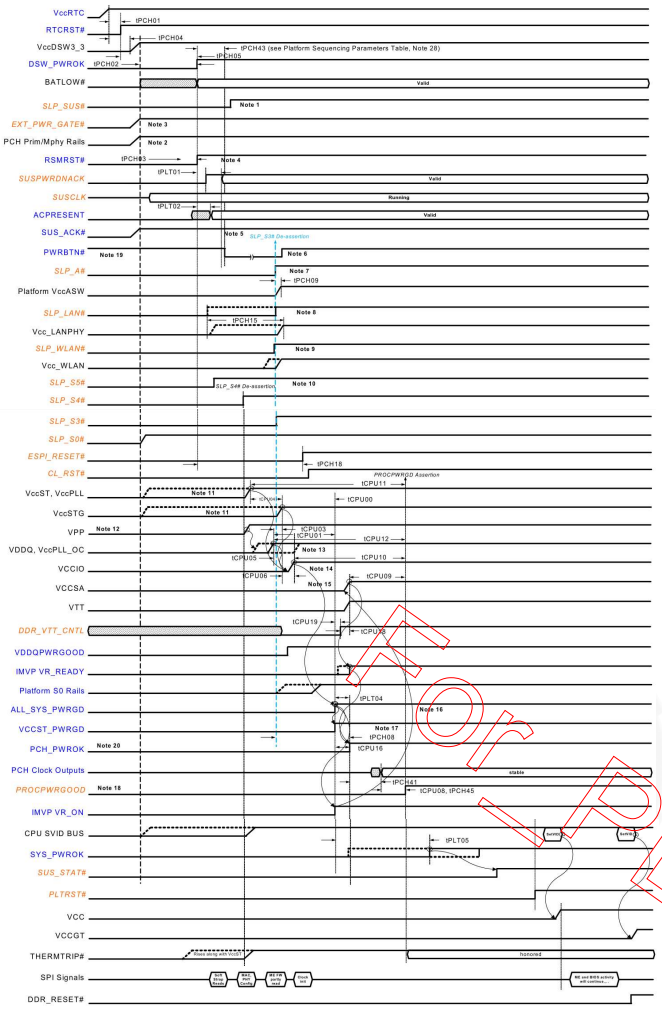
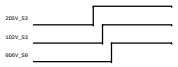
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



For DDR4 power sequence



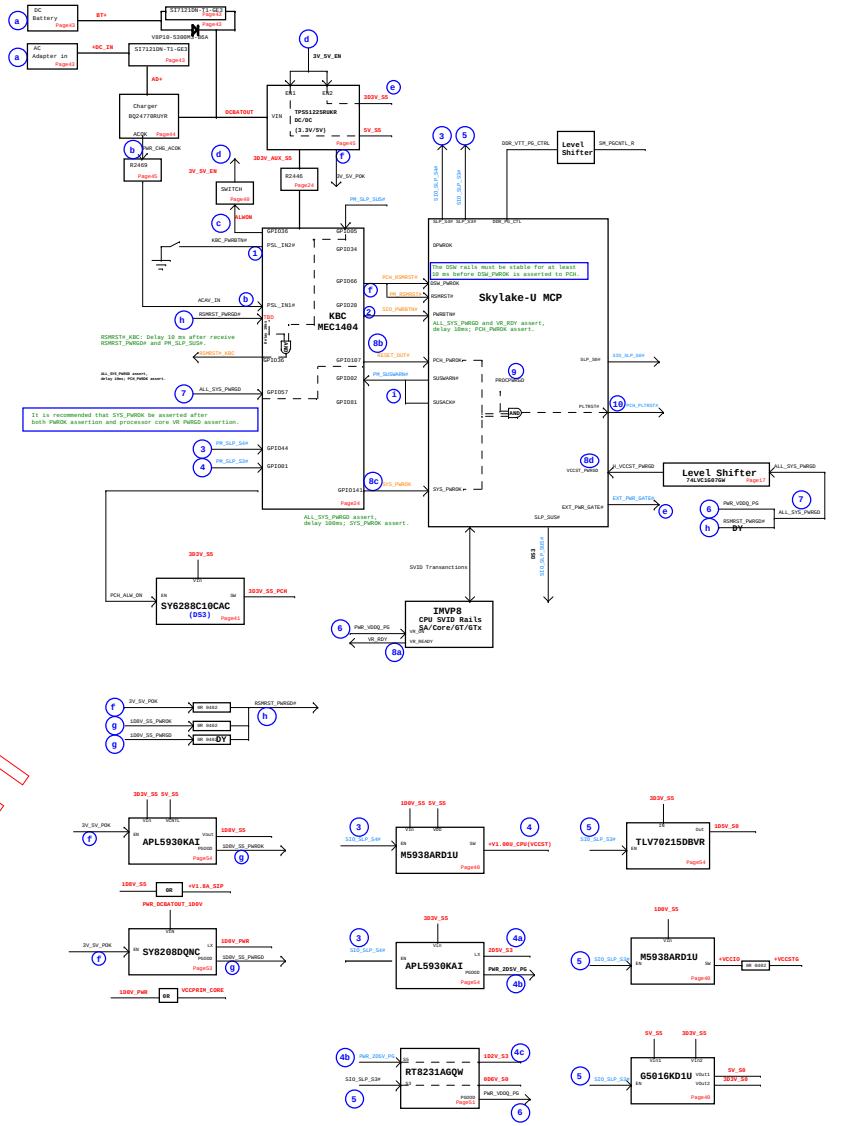
AMD GPU Power sequence

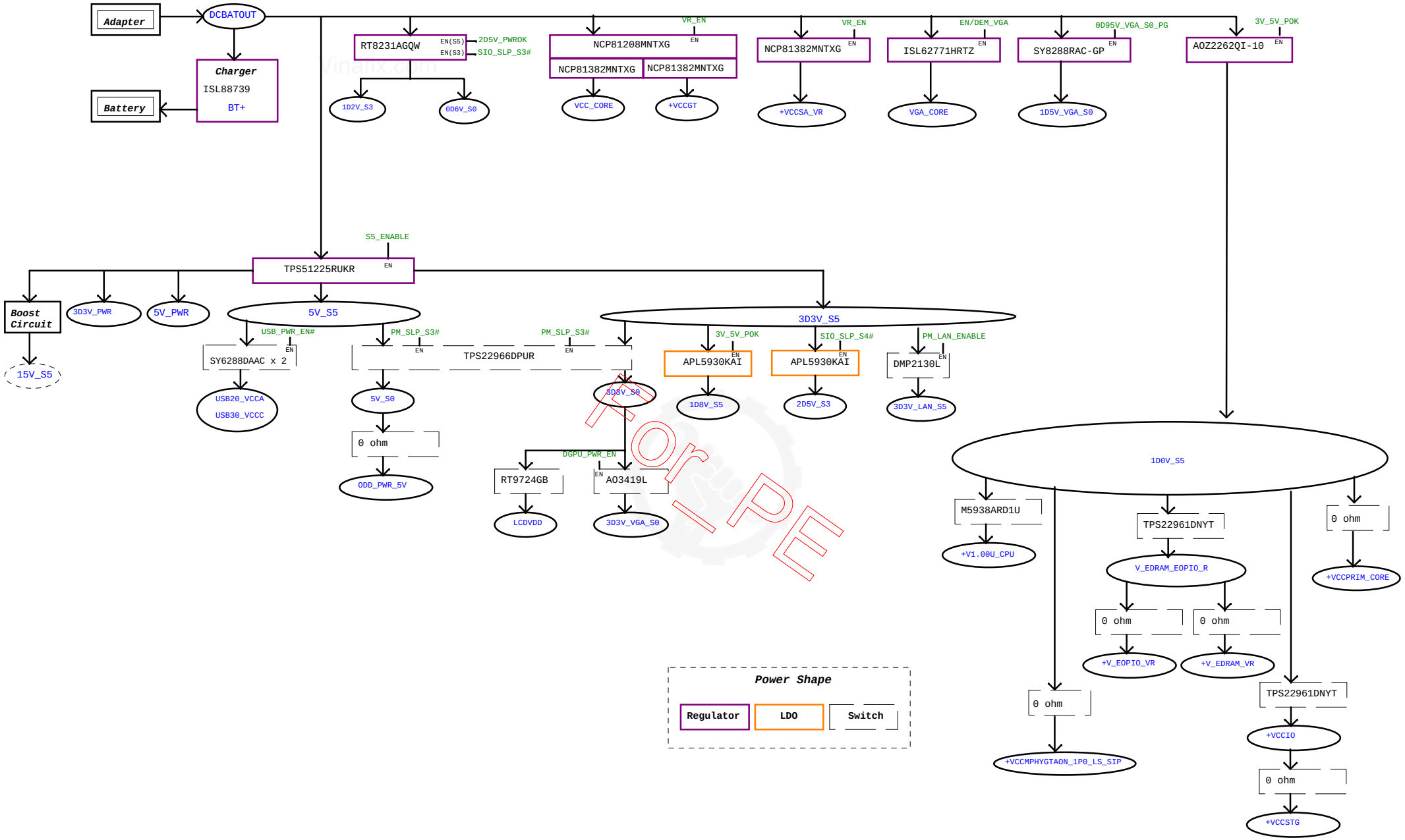
3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D5V_VGA_S0
=> VGA_CORE

20ms
All the ASIC supplies must reach their respective nominal voltages withing of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
It is recommended that the 3.3V rail ramp up first.
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

Red: Power Rail
Orange: Output from KBC
Light Blue: Output from CPU





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Title: Power Block Diagram

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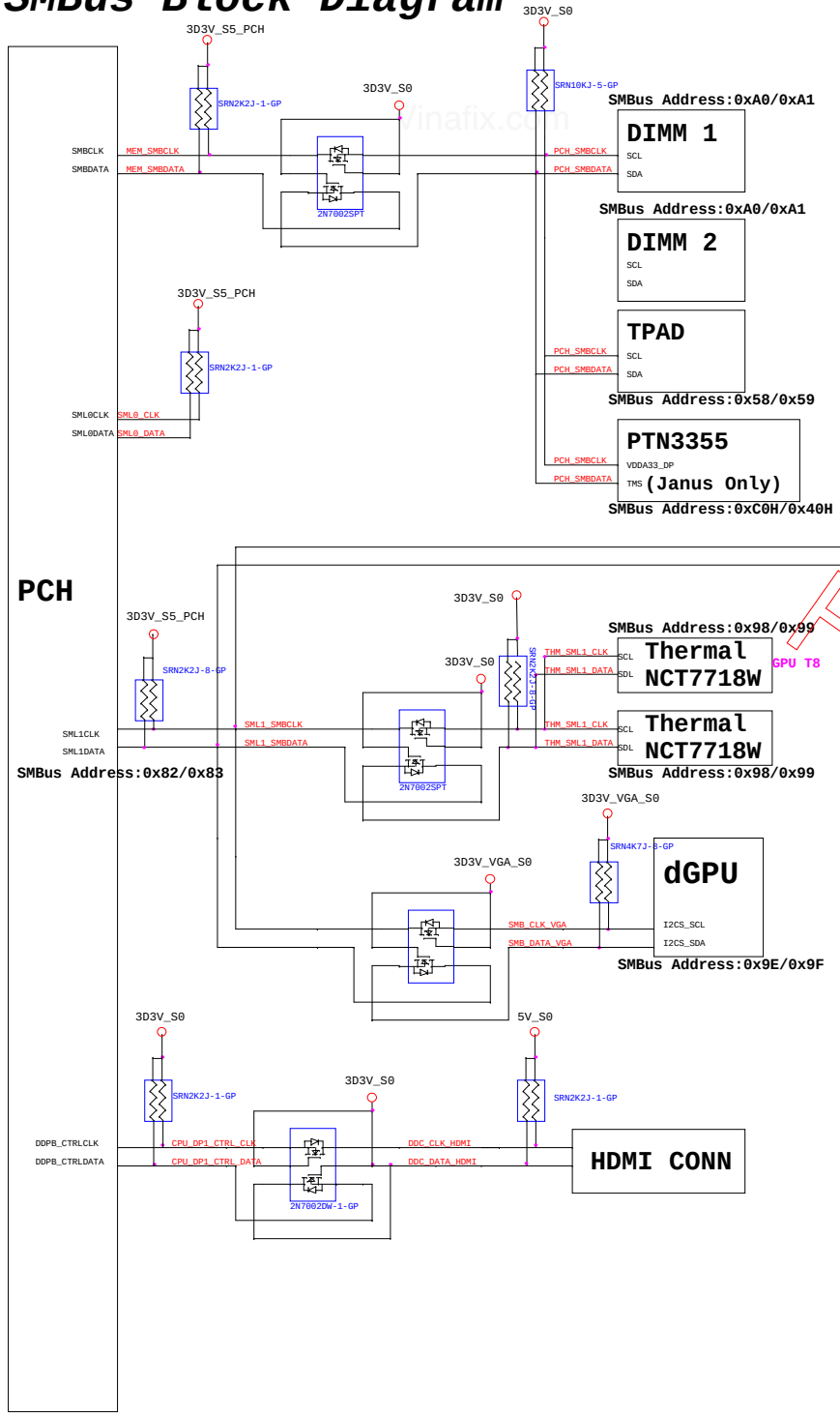
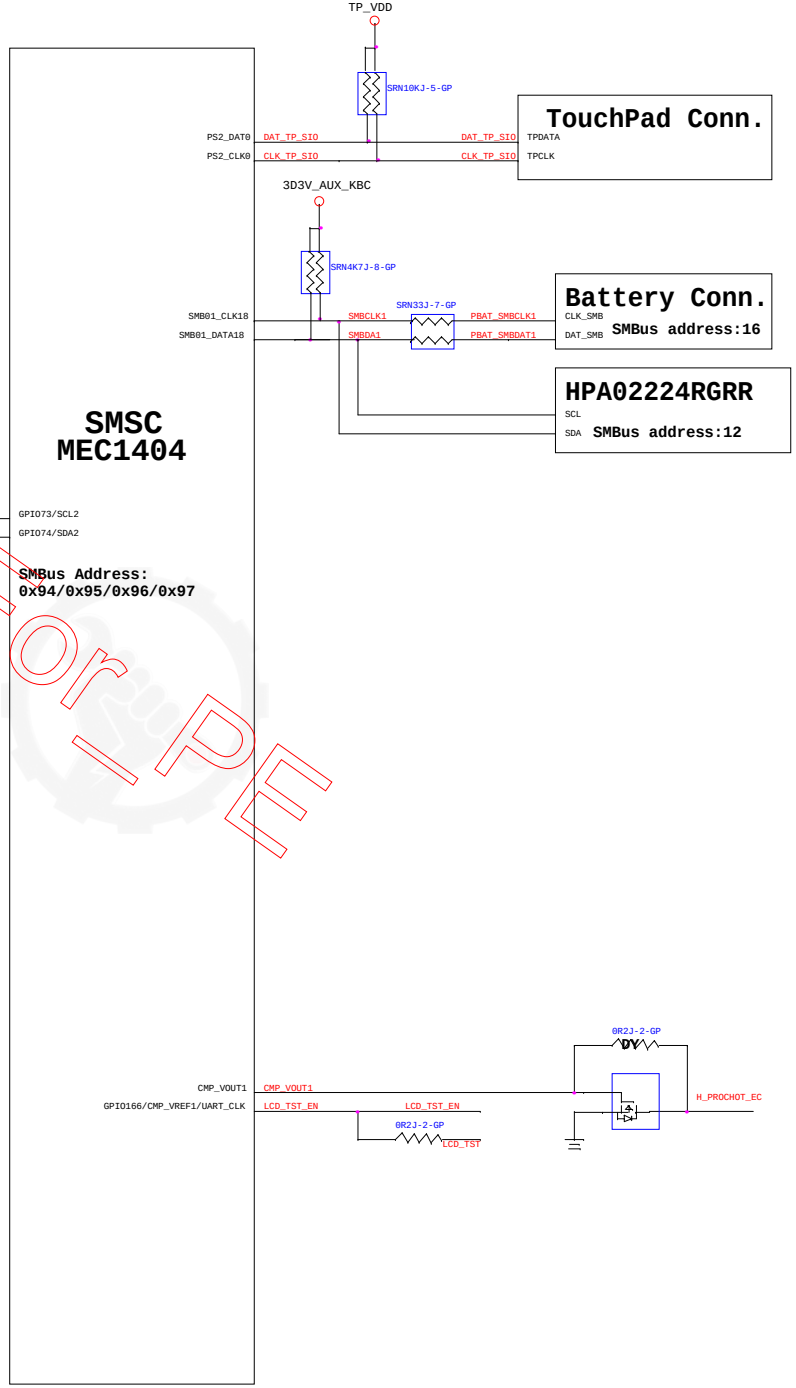
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

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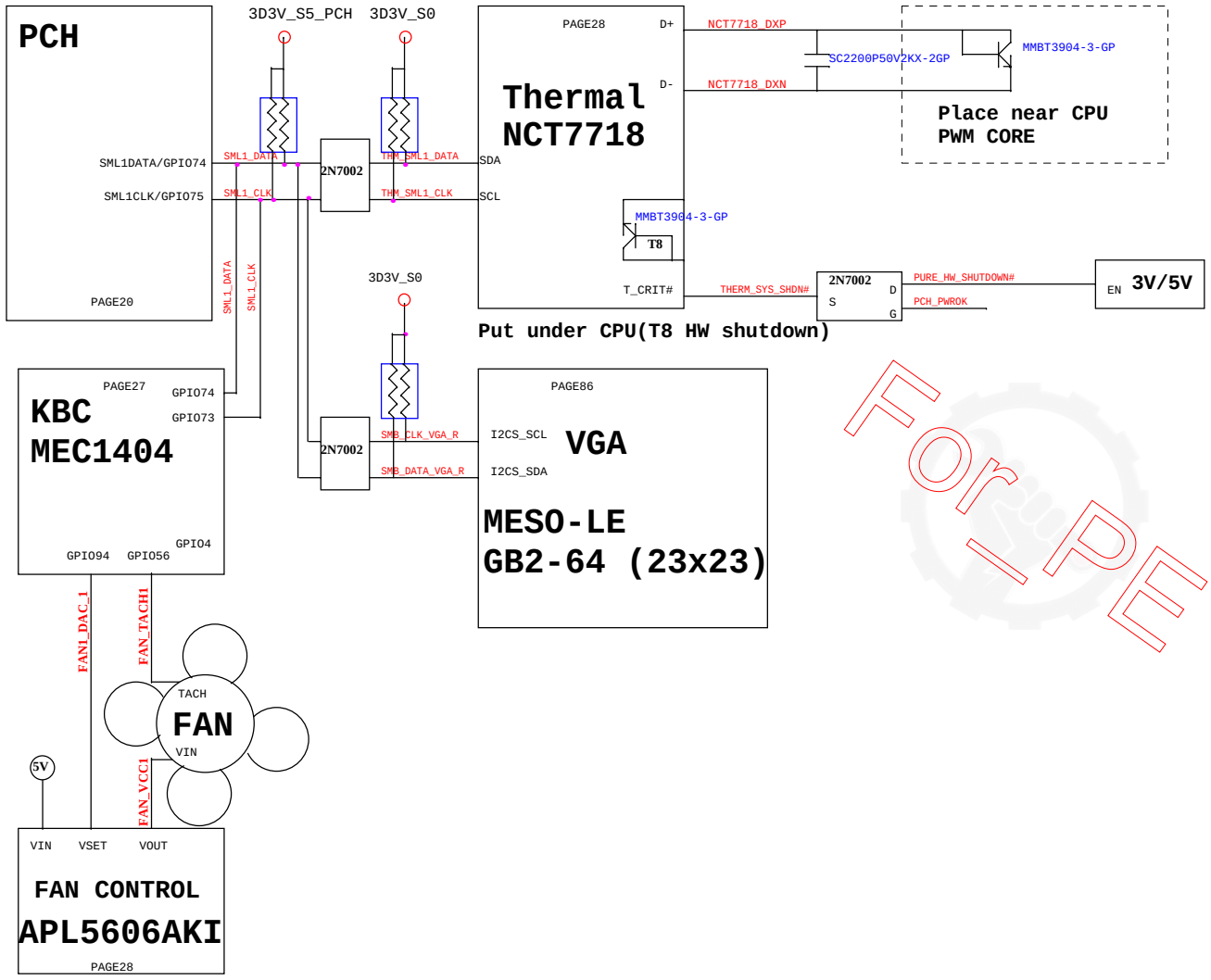
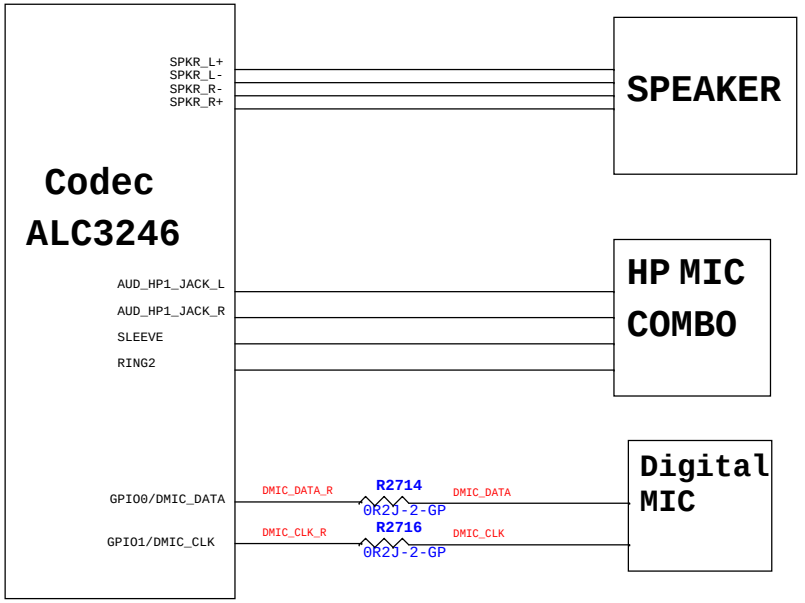
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title	Thermal/Audio Block Diagram	
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